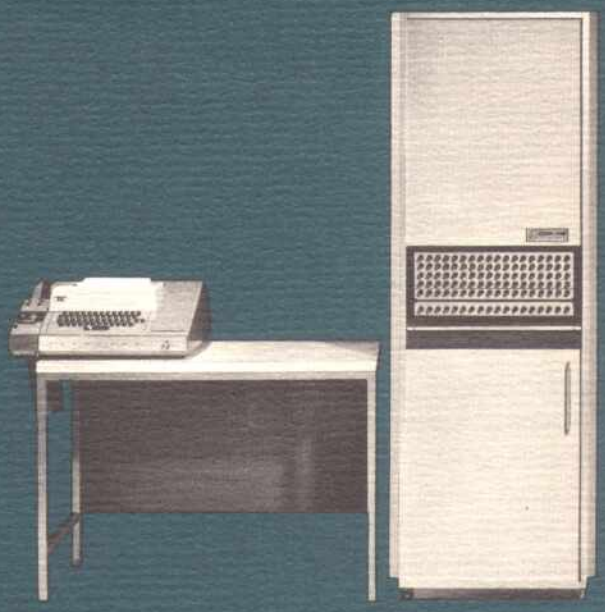


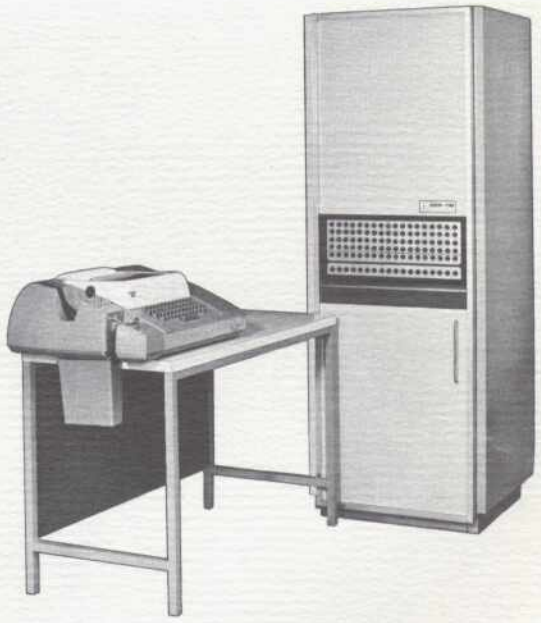
DDP 116

GENERAL PURPOSE DIGITAL COMPUTER

3C COMPUTER CONTROL COMPANY, INC.

FEATURES

- fully parallel machine organization
- sixteen-bit word
- standard 4096 word core memory. 1024 and 8192 modules also available, expandable to 32,768 words
- 1.7 microsecond cycle time memory
- comprehensive instruction repertoire
- complete software package
- FORTRAN
- high proportion of two cycle instructions in typical programs
- most instructions executed in 3.4 microseconds or less, including instruction access and execution time
- I/O bus structure
- standard priority interrupt
- standard keyboard and paper tape I/O unit
- indexing
- high speed arithmetic option
- direct multiplexed channel option
- real-time clock option
- full line of peripherals
- memory parity option
- conservative operation at 2.9 megacycles
- directly compatible with ASCII eight-bit character code
- multi-level indirect addressing
- double length accumulator
- standard I/O includes four sense switches
- powerful set of shift commands
- extensive set of skip branch conditions
- real-time systems interface facility
- individually buffered I/O devices for powerful parallel processing



DDP-116
GENERAL PURPOSE DIGITAL COMPUTER

DDP-116 is a low cost, sixteen-bit binary word general purpose digital computer with a 1.7 microsecond memory cycle time and a standard 4096-word core memory. DDP-116 has a fully parallel machine organization, and both indexing and multilevel indirect addressing. Standard features include a flexible instruction repertoire of fifty-six commands, a powerful I/O bus structure, and standard keyboard and paper tape I/O unit. An extensive programming package including a symbolic assembler and diagnostic and utility routines are included in the DDP-116 basic price. Options include memory parity, a high speed arithmetic option, direct multiplexed channel, direct data channel, a real time clock and a full line of peripheral equipment.

The DDP-116 sixteen-bit word, allows a straightforward and efficient addressing scheme. Most internal operations can be performed in two cycle times (3.4 microseconds), including instruction access and execution time. 1024 words can be addressed by a single word instruction. The sixteen-bit word is directly compatible with the ASCII eight-bit character code.

The DDP-116 is designed for both open-shop scientific applications and real-time on-line data processing and control. Modular design, a flexible I/O structure and command repertoire enable the DDP-116 to be tailored to a broad variety of applications both on and off line. These include data reduction, process control, instrumentation, simulation and open-shop scientific and engineering computation.

SPEED

A basic memory cycle of 1.7 microseconds, single word addressing, flexible instruction repertoire, and a variety of high speed hardware options permit DDP-116 to be used for high speed scientific/engineering computing as well as for real-time control. DDP-116 is capable of 294,000 computations per second. Options permit input and output to occur asynchronously and to be interleaved with processing. Programmed multiplications are performed in 255 microseconds. Divisions take 353 microseconds. With high speed hardware options, these times can be improved to less than 9.5 microseconds for multiplications and 17.9 microseconds for divisions.

PROGRAMMING/USER SERVICES

DDP-116 command structure is flexible and straightforward. A complete programming package including an assembler and comprehensive utility and diagnostic routines come with the standard DDP-116. FORTRAN is under development.

Programmer and maintenance training, a user information service program and installation are all part of the DDP-116 user support program.

EXPANSION

The DDP-116 core memory is optionally expandable to 32,768 words. Memory is available in 1024, 4096, and 8192 word modules.

RELIABILITY

DDP-116 parallel machine organization has permitted use of moderate speed circuitry and wide reliability performance margins.

DDP-116 is constructed with S-PAC digital logic modules. Continuous life test programs with S-PAC modules have proven their extremely high reliability. Life test data available upon request.

SPECIFICATIONS

TYPE

binary, core memory, parallel, single address with indexing and indirect addressing

WORD LENGTH

16 bits; 2's complement arithmetic

SPEED

Add 3.4 microseconds
Multiply (subroutine) 255 microseconds
Multiply (hardware option) 9.5 microseconds
Subtract 3.4 microseconds
Divide (subroutine) 353 microseconds
Divide (hardware option) 17.9 microseconds

MEMORY

1024, 4096* or 8192-word basic modules expandable up to 32,768 words maximum
1.7 microsecond cycle time

INPUT/OUTPUT

ASR 33 teletype unit providing capability for:
- reading paper tape at 10 cps
- punching paper tape at 10 cps
- printing at 10 cps
- keyboard input
- off-line paper tape preparation, reproduction and listing

16-bit input bus
16-bit output bus
priority interrupt
external control and sense lines

SIGNAL LEVELS

Zero volts for logical zero; −6 volts for logical one. All inputs are diode coupled/isolated; all output signals are clamped.

*Standard

CONTROL PANEL

Manual data entry and display of all registers, operational controls, maintenance panel for detection of system malfunction.

SOFTWARE

FORTRAN — Compatible with FORTRAN language as defined by the American Standards Association is under development.

DAP-116 — Symbolic assembly program featuring relocatability, subroutine linkage and allowing FORTRAN compatibility

COP-116 — DDP-116 Check-Out Package — comprehensive program debugging tool.

IOS — Input Output Selector — interprets general input/output requests and processes them according to the I/O capabilities of the specific hardware configuration

A complete set of utility and service routines is provided.

INSTALLATION

The basic computer including a 1024, 4096, or 8192 word memory will be housed in a single rack with the control console mounted on the rack and the ASR 33 mounted beside the computer.

Power: single phase, 115 volt ±10 volts, 60 cps
Operating temperature: 10°C to 45°C
Humidity Range: to 90%
Requires no special wiring, subflooring or other special installation preparation

POWER

Regulated power supplies are included in the DDP-116; no additional regulation is required if input power is within the stated specifications. Overall supply voltage variations due to worst-case combinations, input line voltage changes, dc load regulation, dynamic load regulation, ripple, long term drift, etc., are less than 2% (well within the ±10% circuit tolerances).

INTERNAL ORGANIZATION

PROGRAM COUNTER (P) — Contains location of the next instruction to be performed. Its content is incremented by one each time a new instruction is fetched from the memory and may be incremented an additional time during the execution of a skip command.

MEMORY ADDRESS REGISTER (Y) — Contains the location in memory from which an instruction, an address, or data is to be read.

MEMORY — A coincident current magnetic core memory capable of operating with a 1.7 μsecs cycle time.

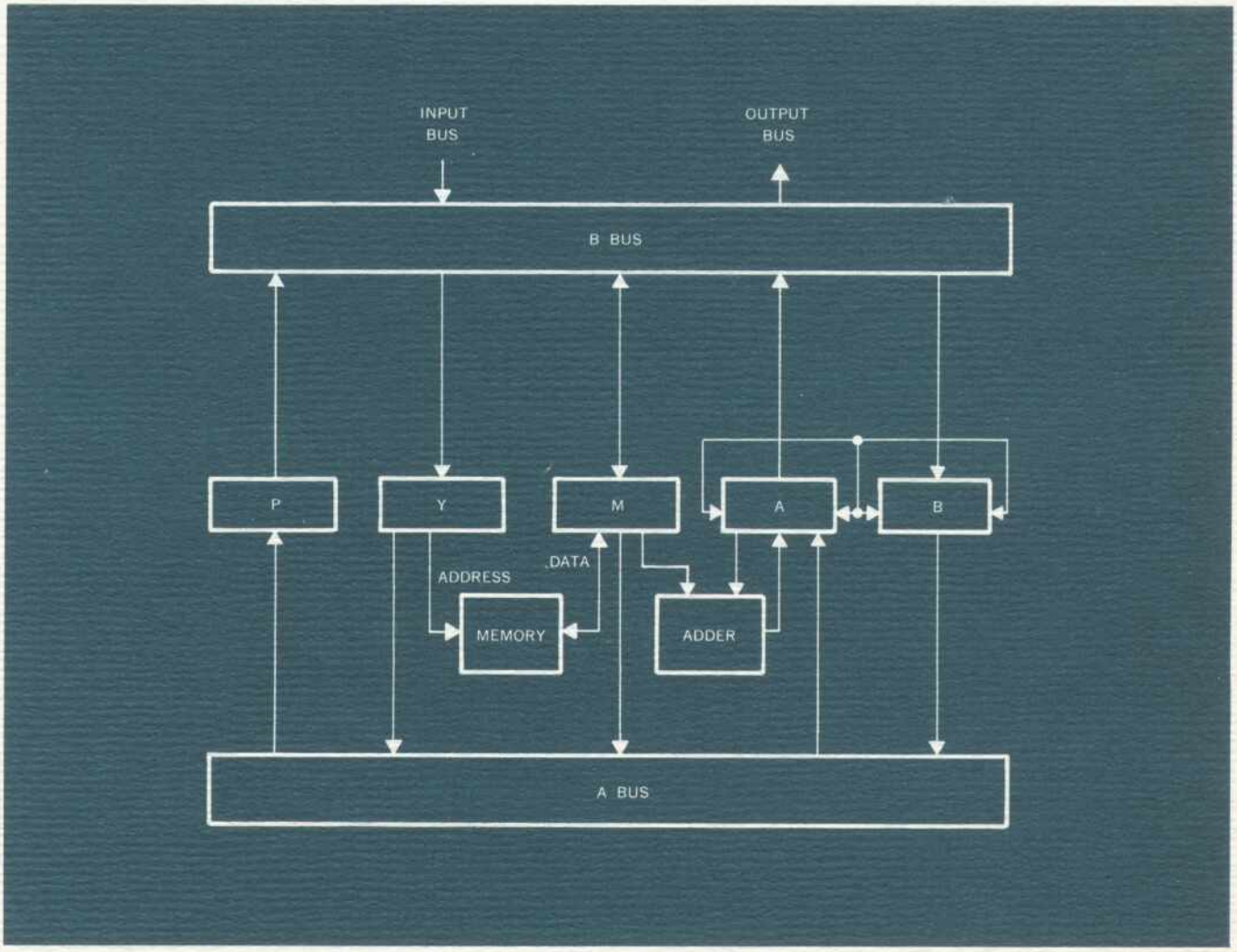
MEMORY INFORMATION REGISTER (M) — Used to hold instructions or data after they have been read out of the memory or before they are read into the memory.

A REGISTER (A) — The principal arithmetic register of the computer. It is used to store the results of arithmetic and logical operations.

B REGISTER (B) — The secondary arithmetic register is used as temporary storage and to hold arithmetic operands which exceed one word in length.

ADDER — Performs the basic arithmetic processes of addition and subtraction.

A BUS AND B BUS — Provide the data transfer paths for moving information between registers.



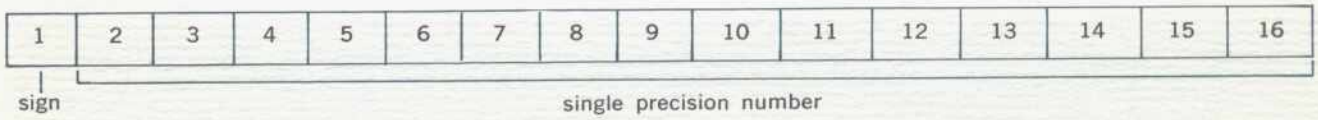
WORD FORMATS

Instruction Format — Memory Reference Instructions

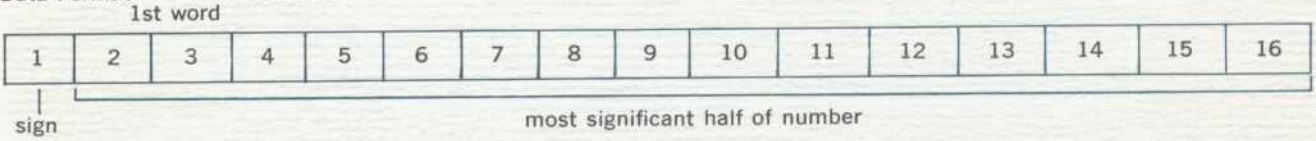
Instruction Format — Non-Memory Reference Instructions

Indirect Address Format

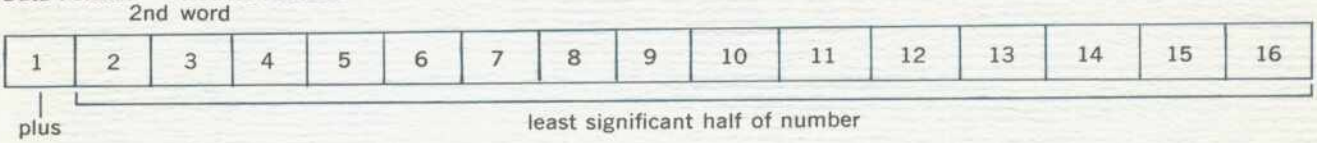
Data Format Single Precision



Data Format — Double Precision
1st word



Data Format — Double Precision
2nd word



ADDRESSING MODES

Memory is divided into sectors of 512 words each

SECTOR ADDRESSING (ONE WORD PER INSTRUCTION)

When the sector flag is a one, the address portion of the instruction refers to the same sector as that addressed by the program counter.

When the sector flag is a zero, the address portion of the instruction refers to sector zero

INDIRECT ADDRESSING

When indirect addressing is required, the effective address is assumed to be in the location specified by the address portion of the instruction and the selected sector address. However, if the location specified by the address portion of the instruction and the selected sector address also calls for indirect addressing, another cycle of indirect addressing is initiated. This chaining of indirect addresses can continue indefinitely for all instructions which permit indirect addressing. Each indirect address cycle requires an additional 1.7 microseconds for instruction execution.

INDEXING

When the index bit is set, the contents of the index register (memory location 0) is added to the effective address of the instruction to produce a new effective address. If indexing is specified in a given instruction, it occurs before any indirect addressing occurs. If indexing is specified in an indirect address, it occurs before any further indirect addressing occurs. When indexing is used, an additional 2.04 microseconds is required for instruction execution.

PRIORITY INTERRUPT

The standard priority interrupt system consists of a single interrupt line to which multiple interrupt sources can be connected. When an interrupt occurs the program counter is stored and control is transferred to a standard location. A software routine then sorts out the source of the interrupt and transfers to the correct subroutine. Interrupt sources can be enabled and inhibited individually under program control. Thus the system permits multiple priority interrupt levels with the stacking of interrupts upon interrupts. Assignment of the priority level of a particular source is also under program control.

INSTRUCTION REPERTOIRE

(Execution times include instruction and operand access)

TYPE	MNEMONIC	TIME	DESCRIPTION
Load and Store	LDA	3.4 μsecs	Load A
	IMA	5.1	Interchange Memory and A
	IAB	1.7	Interchange A & B
	CRA	1.7	Clear A
	STA	3.4	Store A
Arithmetic	ADD	3.4	ADD
	SUB	3.4	SUB
	IRS	5.1	Increment, Replace Memory and Skip
Logical	ANA	3.4	AND To A
	ERA	3.4	Exclusive OR To A
Shift	LGL	1.7 + .34 n	Logical Left
	LGR	1.7 + .34 n	Logical Right
	ALR	1.7 + .34 n	Logical Left Rotate
	ARR	1.7 + .34 n	Logical Right Rotate
	ALS	1.7 + .34 n	Arithmetic Left
	ARS	1.7 + .34 n	Arithmetic Right
	LLL	1.7 + .34 n	Long Left Logical
	LRL	1.7 + .34 n	Long Right Logical
	LLR	1.7 + .34 n	Long Left Rotate
	LRR	1.7 + .34 n	Long Right Rotate
	LLS	1.7 + .34 n	Long Arithmetic Left
	LRS	1.7 + .34 n	Long Arithmetic Right
Transfer of Control	JMP	1.7	Unconditional Jump
	JST	5.1	Jump & Store Location
	CAS	5.1	Compare Memory & A
	SPL	1.7	Skip If A Sign Plus
	SMI	1.7	Skip If A Sign Minus
	SZE	1.7	Skip If A Zero
	SNZ	1.7	Skip If A Non Zero
	SLZ	1.7	Skip If LSB A Zero
	SLN	1.7	Skip If LSB Non Zero
	SSC	1.7	Skip If C BIT Set
	SRC	1.7	Skip If C BIT Reset
	SS 1	1.7	Skip If Sense Switch 1 Set
	SS 2	1.7	Skip If Sense Switch 2 Set
	SS 3	1.7	Skip If Sense Switch 3 Set
	SS 4	1.7	Skip If Sense Switch 4 Set
	SR 1	1.7	Skip If Sense Switch 1 Reset
	SR 2	1.7	Skip If Sense Switch 2 Reset
	SR 3	1.7	Skip If Sense Switch 3 Reset
	SR 4	1.7	Skip If Sense Switch 4 Reset
Input-Output	OCP	3.4	Output Command Pulse
	SKS	3.4	Skip If Ready Line Set
	INA	5.1	Input To A
	OTA	5.1	Output From A
Control	SSP	1.7	Set A Sign Plus
	SSM	1.7	Set A Sign Minus
	CMA	1.7	Complement A
	CSA	1.7	Copy Sign to C BIT & Set A Sign Plus
	ACA	1.7	Add C To A
	SCB	1.7	Set C BIT
	RCB	1.7	Reset C BIT
	HLT		HALT
	NOP	1.7	No Operation
	ENB	1.7	Turn Program Interrupt On
	INH	1.7	Turn Program Interrupt Off

COMMAND STRUCTURE

The DDP-116 command structure is unusually powerful for a machine of its size. Featured are a compare instruction which provides a three-way branch and an increment memory and skip on zero. The latter instruction permits any location in memory to be used as a counter with the test for overflow combined with the basic increment instruction. The shift commands provide the capability for a full set of left or right rotates and shifts and double length rotates. Also included are both single and double length arithmetic shifts with overflow detection to permit easy arithmetic scaling.

The skip commands permit testing of several internal conditions plus the conditions of four sense switches. Skip commands are available for either skipping or not skipping on most conditions.

The indirect addressing and indexing system also has a number of powerful features. Indexing may be specified either before or after indirect addressing thus permitting the index register to be used to increment through a block of data where the instruction address is the base address of the block or to provide the base address of a record in a block of data from which various items are addressed by different instruction addresses. The ability to handle multiple levels of indirect addressing allows subroutines to access operands specified in the main program without any address manipulation. This greatly reduces the execution time of short subroutines.

Another command structure feature is the basic input and output commands which test the status of devices with the actual input/output command thus greatly reducing the number of device-status-testing commands required. Also, the input/output instructions do not hang up the computer on input/output waiting for a ready signal thus eliminating a possible source of problems in real-time systems.

INPUT/OUTPUT

The basic I/O system of the 116 consists of a general input/output bus. This bus is used to transfer a full word in and out of the computer. In addition it contains lines which provide timing signals and commands to peripheral devices. Each peripheral device which is tied to the I/O bus has its own buffer and control logic. This feature permits a high degree of flexibility in using multiple devices concurrently and in handling multiple devices through priority interrupt.

There are four basic modes in which data can be transferred back and forth between peripheral devices of the 116.

a. single word transfer
b. single word transfer with priority interrupt
c. direct multiplexed channel
d. direct data channel

SINGLE WORD TRANSFER MODE

The basic input/output mode of the standard computer is single word transfers under program control. In this mode, words can be read in from external devices into the accumulator utilizing INA instructions, and full words can be transferred from the accumulator to the output device using OTA instructions. During input in this mode, the programmer has the option of clearing or not clearing the accumulator before each input (INA) instruction. This allows input characters to be packed into words as part of a basic input routine. In order to make the 116 extremely flexible in real-time applications, the ability to test and skip on the ready status of an I/O device has been included in the basic input and output instructions. Thus the computer is not required to sit in an input or output instruction waiting for a ready signal. In applications where it is permissible to tie up the computer while performing input or output, quite high data rates can be achieved with this mode. For example, input from magnetic tape option can be performed at tape character rates in excess of 62.2 kilocycles utilizing this mode. This mode is also very convenient for slower devices such as paper tape equipment and card equipment.

SINGLE WORD DATA TRANSFER WITH PRIORITY INTERRUPT MODE

The basic priority interrupt system can also be utilized with the basic input/output commands to provide a powerful input/output mode for relatively slow devices. In this mode frequent testing of a device for readiness is eliminated. The device ready signal causes a program interrupt. The I/O functions are then performed whereupon the program continues in its normal fashion.

DIRECT MULTIPLEXED CHANNEL

A direct multiplexed channel mode is available which permits data transfer between peripheral devices and the memory concurrent with computation. In this mode the starting location to which the block of information is to be transferred and the final location at which the block transfer is to be terminated are set up under program control. The data transfer is then initiated by the program. Once this has been done, transfers occur independent of program control until the specified block of memory has been filled.

Since the starting and final locations of the block of memory are stored in standard locations in memory, this is an extremely economical mode of I/O. Up to eight devices can be connected to the DMC system simultaneously, independently transferring data between each device and a specified block in memory. Because this mode requires only 6.8 microseconds of computer time for each word transfer, a maximum word rate of over 145 kilocycles can be obtained if computation is effectively halted. For slower word rates, any time not needed by the DMC is used by the computer for computation.

DIRECT DATA CHANNEL

A direct data channel system is provided which takes only 1.70 microseconds per word transfer. This is less economical than the Type A system since the starting and final address for the block transfer requires individual registers. However, a maximum transfer rate of greater than 580 kilocycles can be obtained if computation is effectively halted.

INPUT/OUTPUT CONTROL

Peripheral equipment in the 116 is controlled utilizing the OCP and SKS instructions. The OCP instruction permits commands to be sent to peripheral equipment indicating the mode in which they are to operate. The SKS instruction permits the condition of the device to be tested under program control.

In addition to these two basic control commands, actions in the peripheral equipment can be initiated in conjunction with the output from A (OTA) and input to A (INA) commands. These later commands can also test the condition of a device.

DDP-116		INPUT/OUTPUT		PERIPHERAL EQUIPMENT	
STANDARD	OPTIONAL	STANDARD	OPTIONAL	STANDARD	OPTIONAL
• Indexing • 4096-word memory • Indirect addressing • Control and maintenance panel • Complete programming package • Support service	• 1024, 4096, 8192-word memory modules • Memory expansion to 32,768 words • High speed arithmetic unit • Parity • Real-time clock • Automatic power failure protection	• Interrupt line • Direct I/O data transfer to arithmetic register • Full word I/O bus • External Function Bus	• Direct Multiplexed channel • Direct Data channel • Multilevel priority interrupt lines • I/O buffered channels	• ASR-33 teletype unit providing capability for: reading paper tape at 10 cps, punching paper tape at 10 cps, keyboard input off-line paper tape preparation, reproduction and listing	• Paper tape reader 300 ch/sec • Paper tape punch 110 ch/sec • Magnetic tape unit/1 tape transport 45 ips • Magnetic tape unit/4 tape transport 45 ips • Magnetic tape unit/1 transport 75 ips or 112 ips • Card readers • Card punches • High speed line printer • Digital plotter

POWER FAILURE PROTECTION

The standard DDP-116 memory is protected against AC power failure as a standard feature. The memory will automatically shut down without destroying any information when AC power fails. An option is provided which causes an interrupt on power failure permitting the storing of the status of the machine before power goes off. The option also permits automatic restart when power returns.

CONSOLE FUNCTIONS

Displaying and altering all major registers

Entering information in memory

Displaying locations in memory

Single instruction steps

Single cycle steps

Single time pulse steps

Turning power on and off

Displaying machine cycles, halt status and interrupt status

INTERNAL OPTIONS

ARITHMETIC OPTION

Multiply	< 9.5 microseconds maximum
Divide	< 17.9 microseconds maximum
Normalize	

PRIORITY INTERRUPT OPTION

A multi-level priority interrupt system requiring a minimum amount of programming is provided as an option. This system is available in an initial group of seven, succeeding groups of eight to a total of sixty-three. When an interrupt occurs in this system, the program counter is stored in a specific location associated with the particular interrupt line and control is transferred to another standard location. Included in the system is a program controlled mask register which permits individual interrupt lines to be enabled and disabled under program control. This allows priority interrupts to be pyramided on top of other interrupts without an extensive executive routine.

DIRECT MULTIPLEXED CHANNEL

A time shared direct multiplexed channel system is provided as an option. This permits up to eight input/output devices to concurrently transfer information to or from the memory without program intervention. 6.8 microseconds are required for each word transfer; thus giving a maximum rate in excess of 145 kilocycles when computation is halted. This system is extremely economical since the location register and final address register for each device connected to the DMC System are stored in high-speed memory.

DIRECT DATA CHANNEL

This system requires only 1.70 microseconds per word transfer and is thus capable of handling a maximum transfer rate of greater than 550 kilocycles when computation is halted. A hardware location register and range registers are provided with the option.

PARITY OPTION

An optional parity system is available for generating and checking high speed memory parity in a memory module. This option is not normally required because of the extremely high reliability of the computer memory.

REAL-TIME CLOCK OPTION

A real-time clock is available which can be set or read under program control and will cause an interrupt when it reaches zero.

AUTOMATIC POWER FAILURE OPTION

An optional power failure system will permit the computer to save the arithmetic registers and then shut down when a power failure occurs and restart automatically when power returns.

WATCHDOG TIMER OPTION

A watchdog timer is available which can be set under computer control and which sounds an alarm and provides a contact closure when it counts to zero.

PERIPHERAL EQUIPMENT

MAGNETIC TAPE CONTROL UNIT AND TAPE TRANSPORT

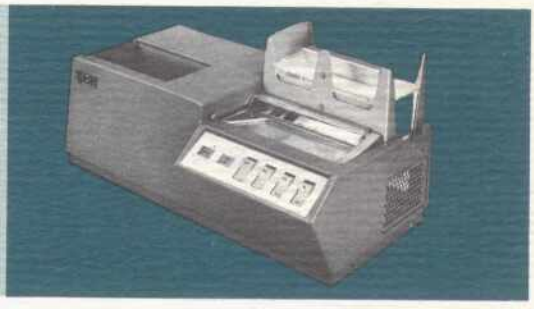
45 ips with 200 or 556 characters/inch recording density with 9 kilocycles or 25 kilocycles data transfer. Control Unit capable of handling up to four Tape Transports. Compatible with IBM 729 Mod II magnetic tapes.

MEDIUM SPEED LINE PRINTER AND ADAPTER

Prints 300 lines per minute, 120 characters per line, 10 characters per inch, 64 characters per drum revolution. Asynchronous input speed to 125 kc. Character synchronization and timing is provided by an eight-channel optical code disc.

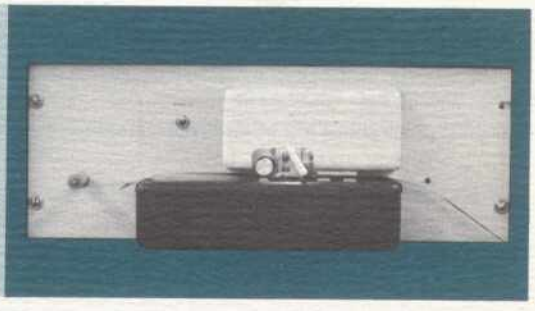
100 CARD-PER-MINUTE CARD READER AND CONTROL UNIT

Reads 100, 80-column punched cards per minute. Provisions are made to select either Hollerith or binary coded information from the Reader.



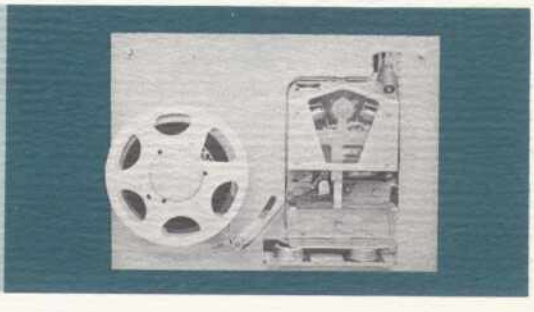
HIGH SPEED PAPER TAPE READER

Uni-directional photoelectric paper tape reader capable of reading 1 inch, 8-level perforated tape continuously at a speed of 300 characters per second; or to step asynchronously at speeds up to 60 characters per second.



HIGH SPEED PAPER TAPE PUNCH

Capable of punching 1 inch, 8-level paper tape at rates up to 110 characters per second.



PROGRAMMING

FORTRAN

The FORTRAN compiler is under development for the DDP-116. This compiler will provide the power and flexibility of FORTRAN as defined by the American Standards Association.

ASSEMBLY SYSTEM (DAP-116)

DAP-116 is a two pass assembly program which translates programs written in mnemonic code and converts them to the machine language of the DDP-116. The language format conforms to Share Standards and includes all the basic mnemonic instructions plus a variety of pseudo instructions for:

1. allocation of core memory
2. definition of data
3. generation of linkage to library subroutines
4. control of input/output options available

A built-in feature of DAP-116 is the automatic processing of sector addresses. Pseudo operations included in the DAP-116 language are:

ABS	BSS	MOR	NTRI
REL	EQU	DEC	NTRY
BCI	CALL	BSZ	LIST
OCT	ORG	POOL	NLST
BES	END	COMN	

Object programs produced are either absolute or relocatable.

DEBUG PROGRAM (COP-116)

The debug program is a compact relocatable program capable of:

1. Typing memory in octal
2. Punching memory in loader format
3. Modifying memory using the typewriter keyboard
4. Entering breakpoints into a program
5. Clearing to zero all or part of memory
6. Initiating jumps or halt jumps to any part of memory
7. Searching all or part of memory for a specified address
8. Halting during program execution on any memory address referenced by the program becoming equal to a prestored parameter
9. Printing out an object tape in loader format

DIAGNOSTICS

An extensive diagnostic package is provided with the DDP-116, which includes routines for verifying the operation of the control unit, arithmetic unit, core memory, and the available input/output devices. These routines generate indicative information reflecting the operational status of the equipment being verified.

DUMP

DUMP is a compact relocatable program which enables the user to obtain memory dumps in octal or mnemonic instruction format. The program is completely modular. Each function available is provided in subroutine format, i.e., if the user desires only an octal memory dump, he need only carry the coding necessary to perform this function. The DUMP can communicate with any output equipment available in the system through the Input/Output Selector Program.

LOADER

The loader is a relocatable program which loads the memory with octal information in absolute or relocatable format. This program is capable of loading the main program or subroutine called by other subroutines and completes the transfer vector linkage between the main program and external subroutines. Also included is the capability to load special indirect address words into sector zero. These words are generated by the assembly program.

SIMULATOR

The DDP-116 simulator is a DDP-24 program which interprets and executes instructions written in DDP-116 code utilizing the ASR-33 Input/Output equipment. DDP-116 programs may be checked out or run operationally on either DDP-24 or DDP-224 computers.

SUBROUTINES

Double Precision Arithmetic	— add, subtract, multiply and divide
Fixed Point	— sine, cosine, arctan, log, exponential, square root
Conversion	— binary to BCD BCD to binary
Single Precision	— multiply and divide

INPUT/OUTPUT SELECTOR

A powerful input/output program which establishes the input/output communication links for systems or main programs with input/output equipment. IOS provides routines for line image, individual peripheral device, device to device, computer to device, device to computer and integrated peripheral communication. Users with varying complements of peripheral equipment are readily accommodated by the modular design of IOS.

UPDATE

UPDATE is a program which facilitates the deletion, insertion or replacement of source program statements located on paper tape, and whose output is a punched paper tape and/or a listing of the modified tape.

USER SERVICES

Support services, included with purchase of the standard DDP-116, are designed to provide the user with continuing service, training and the benefits of an active User's Group.

PROGRAMMER TRAINING COURSE includes instructions for programming in machine language, an introduction to DDP-116 programming systems, and instruction in DDP-116 operation. One-week course provided quarterly at no cost.

MAINTENANCE TRAINING COURSES include instruction in operation, logic design, diagnostic procedures, diagnostic routines and preventive maintenance. A logistic support program for personnel with previous digital logic design knowledge is included. Two-week courses are conducted semi-annually.

LOGISTIC SUPPORT PROGRAM provides after-delivery service and information to DDP-116 users. Statistical compilation of field operating experience based on a failure reporting program, technical notes on system hardware modification, technical notes on programming modification, spare parts provisioning, and stocking of programming forms and paper tapes are provided.

ADDITIONAL PROGRAMMING, MAINTENANCE AND SYSTEMS ENGINEERING SERVICES are available on a contract basis.

DDP-116
SUMMARY OF OPTIONS AND PERIPHERAL EQUIPMENT

Model Number	Item
116-00	DDP-116 general purpose computer, indirect addressing, indexing, TTY paper tape I/O, page printer, interrupt line, full word I/O bus. 4096 word memory.
116-01	DDP-116 general purpose computer, indirect addressing, indexing, TTY paper tape I/O, page printer, interrupt line, full word I/O bus. 1024 word memory.
116-02	DDP-116 general purpose computer, indirect addressing, indexing, TTY paper tape I/O, page printer, interrupt line, full word I/O bus. 8192 word memory.
116-05	Additional 4096 word memory module.
116-06	Additional 8192 word memory module.
116-07	Memory Module Parity system which generates, stores, and checks parity during memory operation.
116-09	Power failure interrupt and restart system.
116-11	High speed hardware multiply and divide unit.
116-20	DIRECT MULTIPLEXED CHANNEL (DMC). memory controlled.
116-21	DIRECT DATA CHANNEL (DDC). hardware controlled.
116-25	Priority interrupt system with unique memory destinations, interrupt of interrupt, includes 7 interrupt lines.
116-26	Additional group of eight priority interrupt lines with unique memory destinations and interrupt of interrupt.
116-40	Magnetic tape control unit and one transport, 45 ips, 200 and 555 bpi, 25 kc. IBM 729 Mod II compatible.
116-40-1	Magnetic tape control unit and four tape transports, 45 ips. 200 and 555 bpi, 25 kc.
116-41	Magnetic tape control unit and one tape transport, 200 and 555 bpi, IBM 729 Mod II compatible. 75 or 112 ips.
116-50	High speed paper tape reader and control unit, reads at 300 characters per second continuous, 60 characters per second incremental.
116-51	Paper tape spooler.
116-52	High speed paper tape punch and control unit, punches at 110 characters per second.
116-60	Card reader, 100 cpm.
116-64	Card punch, 100 cpm.
116-67	Medium speed line printer, 120 columns, 300 lines per minute.
116-70	XY plotter 300 increments per second.

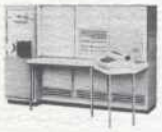
3C GENERAL PURPOSE COMPUTERS

DDP-224

24-bit word DDP-224 features: 1.9 μsecs (0.8 access) memory cycle, and powerful command structure, 260,000 computations per second. Transfer rates up to 325,000 words per second. 3.8 μsecs add. 6.46 μsecs multiply. 17 μsecs divide. 4096-word memory expandable to 32,768. Typical add time with optional floating point hardware 7.6 μsecs (24-bit mantissa, 9-bit characteristic). Fully program compatible with DDP-24.

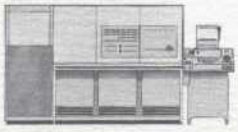
DDP-224 MULTI-PROCESSOR

Fully buffered control unit, access distribution unit and time multiplex unit make it possible to combine several DDP-224's into integrated large scale computer systems with functionally common and/or private memory, control arithmetic, system input/output facilities and peripherals.



DDP-24

DDP-24 features 5 μsecs (2.5 access) memory cycle, powerful command structure, fully parallel machine organization, 100,000 computations per second. Transfer rates up to 166,000 words per second. 10 μsecs add. 30 μsecs multiply. 32 μsecs divide. 4096-word core memory expandable to 32,768. Typical add time with floating point hardware 116 μsecs (24-bit mantissa, 9-bit characteristic).



DDP-24A

A version of the standard DDP-24 which substitutes teletype paper tape and teleprinter I/O for the paper tape reader, punch, and I/O typewriter. Same main-frame features.

DDP-24 VM

The Van Mounted DDP-24 is a rugged, compact, fully mobile general purpose digital computer; functionally identical to the 24 with paper tape reader, punch, and specially mounted I/O typewriter.

DDP-24P

The Portable DDP-24 is being manufactured to offer full computer capability in an ultra-compact configuration to meet demands for shipboard, airborne and other applications requiring portable computer installations.

3C PRODUCTS

S-PAC Logic Modules
200 kc,
1 mc, 5 mc

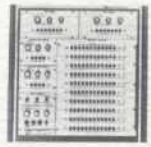
Silicon S-PAC Logic Modules
1 mc

H-PAC Logic Modules
20 mc

Soniline Delay Lines

Magnetic Core Memories

Pulse Current Generators



Digital Program Generators

3C SPECIAL PURPOSE SYSTEMS

Spaceborne

GSE

Military

Industrial

Commercial

Educational

3C DISTRICT OFFICES

New England
670 Hillside Avenue, Rte. 28
Needham, Massachusetts 02194
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449-1861

Long Island
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Commack (L.I.), New York 11725
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265-5567

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8367 Bristol Pike
Levittown, Pennsylvania 19054
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824-5187

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463-4535

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Silver Spring, Maryland 20910
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Orlando, Florida 32809
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COMPUTER CONTROL COMPANY, INC.

WESTERN DIVISION
2217 Purdue Avenue
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Tel: (213) 478-0481
or 272-9135

Printed in U.S.A.

STANDARD DDP-116 PURCHASE PRICE SCHEDULE

Effective 12 October, 1964, Subject to Change Without Notice.

Model Number	Item	Price
116-00	DDP-116 general purpose digital computer with 4096 words of core memory, Teleprinter with paper tape unit, interrupt line and I/O bus system.	$28,500.00
116-01	DDP-116 general purpose digital computer with 1024 words of core memory, Teleprinter with paper tape unit, interrupt line and I/O bus system.	23,500.00
116-05	Additional 4096 words of core memory.	16,000.00
116-06	Additional 8192 words of core memory.	26,000.00
116-11	High speed multiply and divide hardware.*	5,000.00
116-12	Real-time clock.*	1,500.00
116-20	Direct Multiplex Channel and first sub-channel.*	3,500.00
116-20-1	Sub-channel for connecting standard peripheral equipment option to DMC.*	600.00
116-40	Magnetic tape control unit and one tape transport, IBM 729 Mod II compatible, operates at 200 and 555 bpi, 45 ips.	22,700.00
116-40-4	Magnetic tape control unit and four tape transports, IBM 729 Mod II compatible, operates at 200 and 555 bpi, 45 ips.	53,600.00
116-41	Magnetic tape control unit and one tape transport, IBM 729 Mod II compatible, operates at 200 and 555 bpi, 75 or 112 ips.	31,500.00
116-50	High speed paper tape reader, reads at 300 cps.*	3,800.00
116-51	Paper tape spooler.*	1,500.00
116-52	High speed paper tape punch, punches at 110 cps.*	4,500.00
116-60	Card reader, reads at 100 cpm.*	4,500.00
116-64	Card punch, punches at 100 cpm.*	25,000.00
116-67	Medium speed line printer, 300 lpm, 120 columns.	35,000.00
116-70	Digital plotter, 300 ips.	8,400.00
116-91	Enclosure and cooling unit.	600.00
116-92	Power supply.	745.00

*Does not include enclosure or power supply.

F.O.B. Framingham, Mass., Terms Are Net 30 Days.

COMPUTER CONTROL COMPANY, INC., OLD CONNECTICUT PATH, FRAMINGHAM, MASS. 2217 PURDUE AVENUE, LOS ANGELES, CALIFORNIA

STANDARD DDP-116 LEASE PRICE SCHEDULE

Effective 12 October, 1964, Subject to Change Without Notice.

Model Number	Item	Monthly Lease Price Including Maintenance
116-00	DDP-116 general purpose digital computer with 4096 words of core memory, Teleprinter with paper tape unit, interrupt line and I/O bus system.	$ 920.00
116-01	DDP-116 general purpose digital computer with 1024 words of core memory, Teleprinter with paper tape unit, interrupt line and I/O bus system.	750.00
116-05	Additional 4096 words of core memory.	510.00
116-06	Additional 8192 words of core memory.	820.00
116-11	High speed multiply and divide hardware.*	160.00
116-12	Real-time clock.*	50.00
116-20	Direct Multiplex Channel and first sub-channel.*	110.00
116-20-1	Sub-channel for connecting standard peripheral equipment option to DMC.*	20.00
116-40	Magnetic tape control unit and one tape transport, IBM 729 Mod II compatible, operates at 200 and 555 bpi, 45 ips.	720.00
116-40-4	Magnetic tape control unit and four tape transports, IBM 729 Mod II compatible, operates at 200 and 555 bpi, 45 ips.	1,690.00
116-41	Magnetic tape control unit and one tape transport, IBM 729 Mod II compatible, operates at 200 and 555 bpi, 75 or 112 ips.	1,000.00
116-50	High speed paper tape reader, reads at 300 cps.*	120.00
116-51	Paper tape spooler.*	50.00
116-52	High speed paper tape punch, punches at 110 cps.*	145.00
116-60	Card reader, reads at 100 cpm.*	145.00
116-64	Card punch, punches at 100 cpm.*	800.00
116-67	Medium speed line printer, 300 lpm, 120 columns.	1,100.00
116-70	Digital plotter, 300 ips.	265.00
116-91	Enclosure and cooling unit.	20.00
116-92	Power supply.	25.00

*Does not include enclosure or power supply.

F.O.B. Framingham, Mass., Terms Are Net 30 Days.

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