



Pulse

This is the first issue of the 3C Pulse — a periodical written with the busy reader in mind. It will appear from time to time rather than at stated intervals and, its objective is to pass interesting and worthwhile information along to you IN BRIEF FORM. A typical issue may touch on any or a number of the following topics: new products, interesting product applications, areas of mutual interest, names and dates of conventions where 3C will display its products, new Sales Representatives and important personnel additions, pricing information and the like.

3C's CURRENT ADDRESS For those who may not have noticed it, the Eastern Division found it necessary to expand. On July 24, 1959 it moved into a new plant especially designed for it, at 983 Concord Street, Framingham, Mass. It has three times the floor area of its former location. Our Boston telephone number is CEdar 5-6220, while the Framingham number is TRinity 5-6185. You can also teletype us at FRAM MASS 17.

SEVEN NEW M-PACS — TWO NEW T-PACS See attached 3C Pulse numbers 2 and 3 for details, schematic diagrams and prices.

NEW M-PAC PRICE LIST If you cannot find yours (we did make a mailing), we'll gladly send you a replacement. It is dated September 17, and includes all of the latest REDUCTIONS.

3C's FORTHCOMING CONVENTION ATTENDANCES We will display our products in booth #604 at the Northeast Electronic Research and Engineering Meeting (NEREM), Commonwealth Armory, Boston, November 17-19, and in booths #12 & 13, Eastern Joint Computer Conference (EJCC), Statler Hilton Hotel, Boston, December 1-3.

NEW 3C PERSONNEL ADDITIONS Within the past 90 days 3C has appointed T. Ray Henry, Jr., as Contract Administrator, John V. Cockin as Advertising Manager; Leonard H. Eisner, Ara A. Aykanian and Joseph W. Colleran as Application Engineers.

ELECTRICAL DESIGN NEWS — OCTOBER 1959 Did you see the interesting article on pages 28 and 29 entitled "Magnetostriction Transduces Delay Line Signal"? It refers to our LE-10 Logical Element and SM-10 Serial Memory.

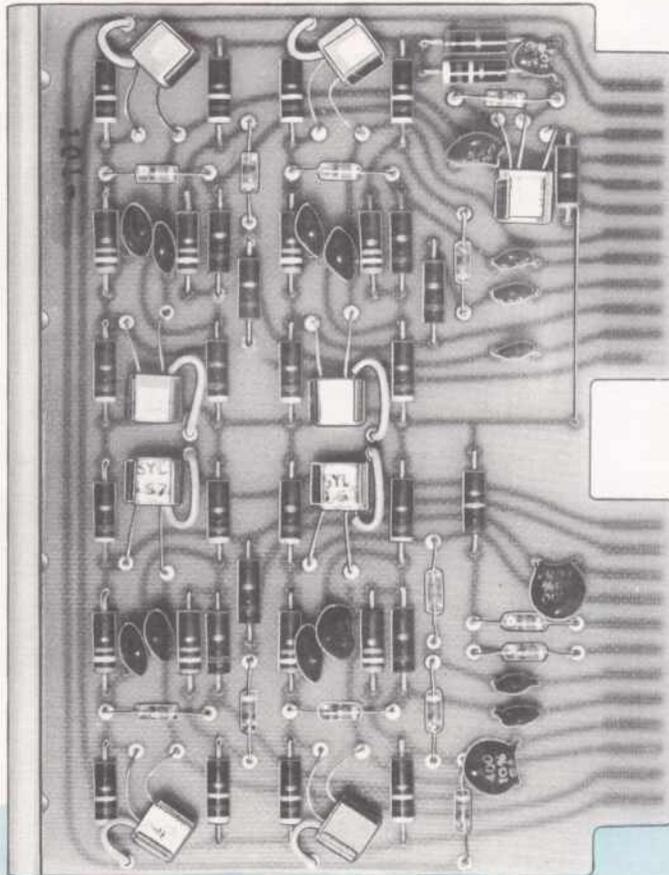
COMPUTER CONTROL COMPANY, INC.

EASTERN DIVISION

WESTERN DIVISION

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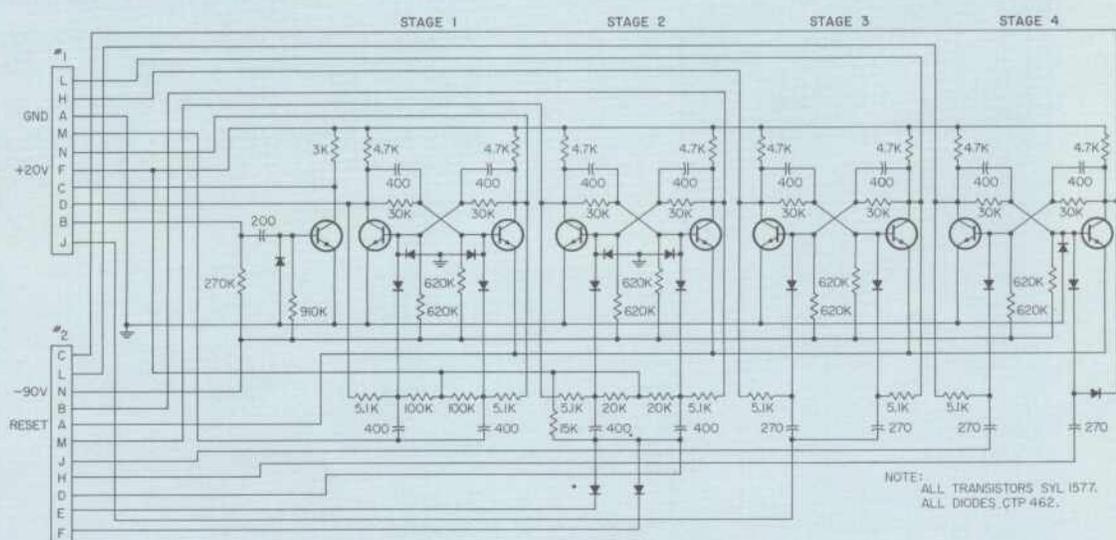
Pulse



BINARY DECADE COUNTER, MODEL BD-101. Model BD-101 consists of four transistor flip-flops that may be externally connected as a binary counter, binary-coded decimal counter, or other multistage counter that requires feedback. Power requirements: +20 volts at 20 ma, -90 volts at 1 ma. Maximum input rate: 100kc.

UNIT PRICE \$99.00

MODEL BD-101



Prices are F.O.B. Framingham, Massachusetts

Net 30 days

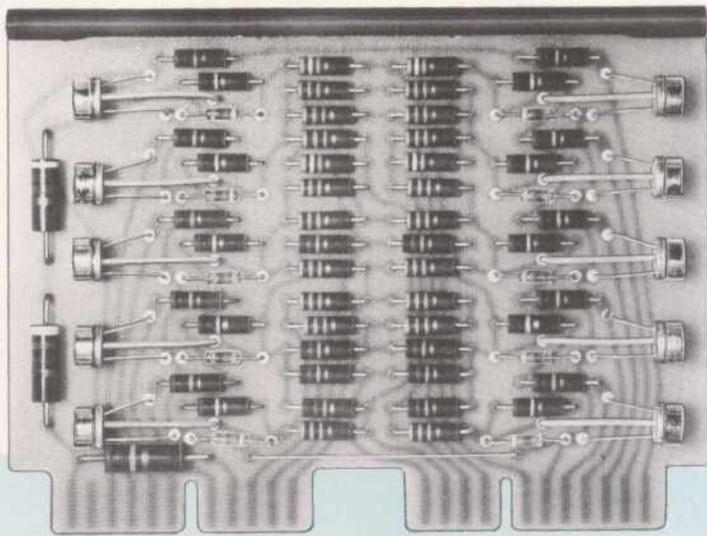
All prices are subject to change without notice.

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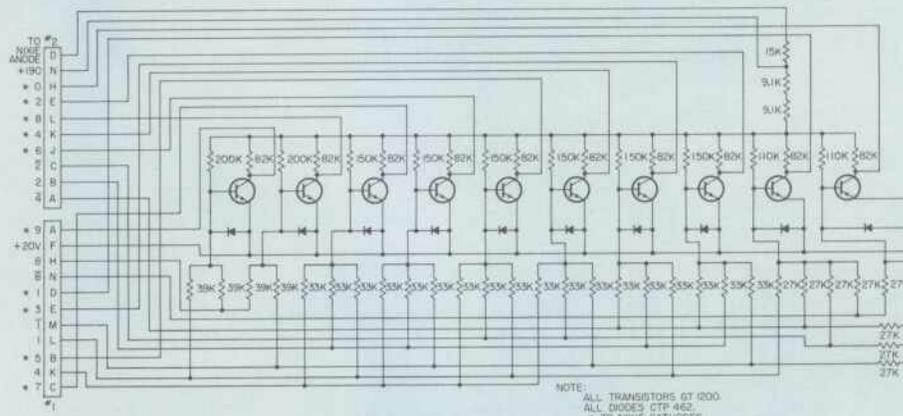
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NIXIE INDICATOR DRIVER, MODEL NX-101. The NX-101 NIXIE Driver is a BCD to decimal converter that accepts the 8-4-2-1 binary decimal code from a BD-101, or equivalent decimal counter, and applies appropriate drive signals to the corresponding cathode of a NIXIE tube. Each of the ten stages consists of an NPN transistor and a resistor decoder. The NIXIE tube is external to the NIXIE Driver and is not included with it. The NX-101 will satisfactorily decode signals from any counter capable of sustaining an additional 3 ma of current in the ON transistor and whose OFF collector potential is at a minimum of +17 volts. Power requirements: +195 volts $\pm 2\%$ at 5.5 ma, +20 volts $\pm 5\%$ at 9.5 ma. Input specifications: +18 volts $\pm 10\%$, -5% at 3 ma. Output specifications: +20 volts at 2 ma.

UNIT PRICE \$134.00

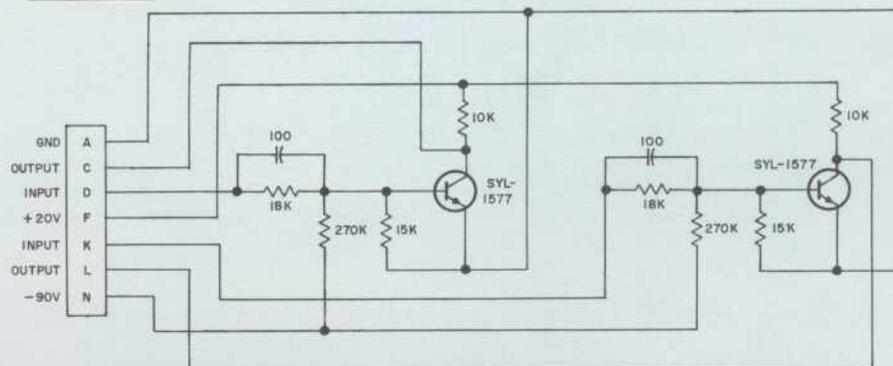
MODEL NX-101



D-C INVERTER AMPLIFIER, MODEL DI-101. Each inverter circuit will drive one M-PAC or up to 5 gate legs. The DI-101 package contains two identical circuits with independent inputs and outputs. Both input and output are direct-coupled allowing cascading of the gates and greater logical versatility by inverting the gate outputs. With the input at ground, the output is approximately +15 volts, depending on the load. When the input is +6 volts or greater, the output goes to ground. Power requirements: -90 volts, 0.5 ma, +20 volts, 1.5 ma.

UNIT PRICE \$34.00

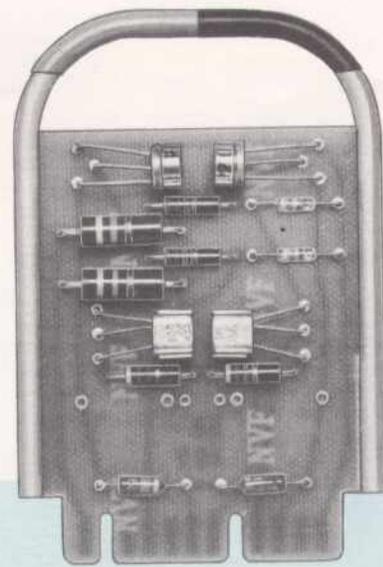
MODEL DI-101



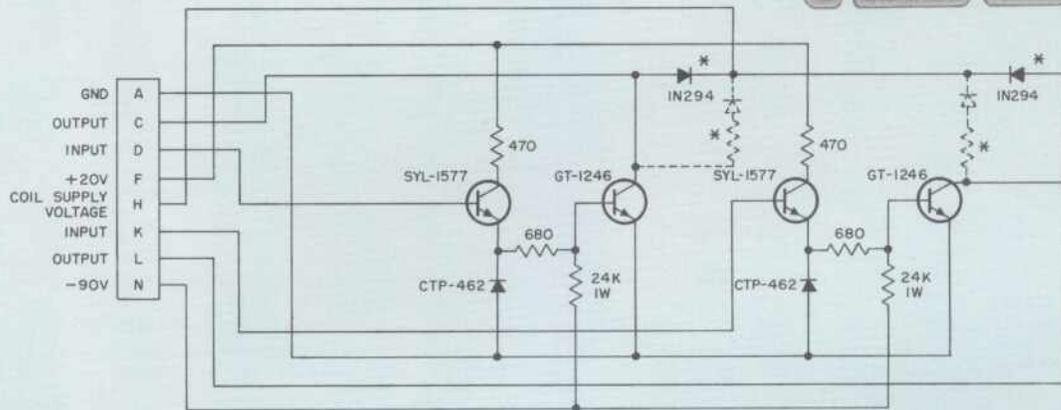


SOLENOID DRIVER, MODEL SD-102. Each Model SD-102 contains 2 independent solenoid driver circuits. Each circuit amplifies the output of a standard M-PAC to drive a solenoid load of up to 50 volts at 150 ma. A diode in each circuit suppresses inductive kick. Power requirements: +20 volts at 12 ma, -90 volts at 4 ma. Input requirements: Approximately 0.5 ma into a 30K input impedance.

UNIT PRICE \$44.00



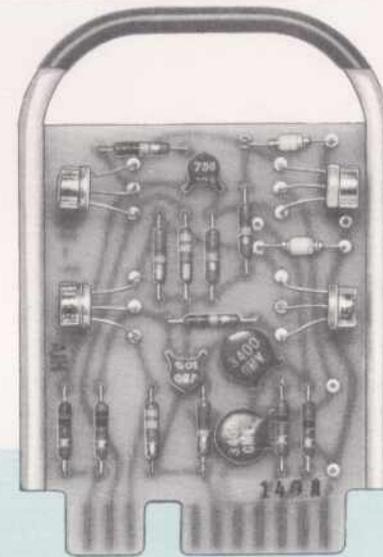
MODEL SD-102



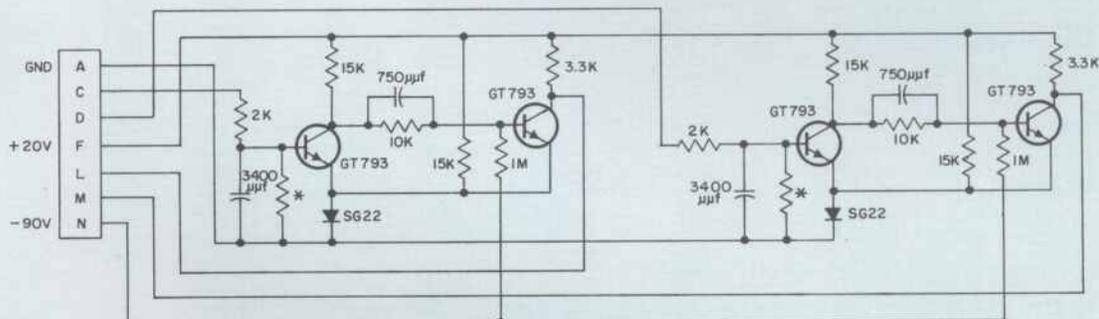
NOTE:
* ALTERNATE CIRCUITS IF FASTER RECOVERY TIME IS DESIRED.

SCHMITT TRIGGER, MODEL ST-102. Model ST-102 contains 2 independent circuits each of which can drive any of the other M-PAC circuits. The output signal switches between +0.7 and +20 volts as the input signal crosses the triggering level. The triggering level is tailored to individual requirements between 1 and 8 volts with an accuracy of ± 0.5 volts. Power requirements: +20 volts at 7 ma, and -90 volts at 0.1 ma.

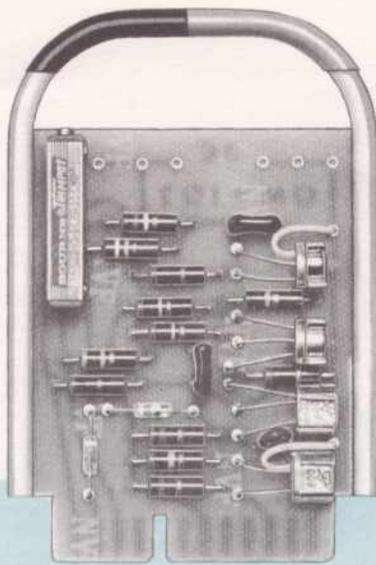
UNIT PRICE \$59.00



MODEL ST-102



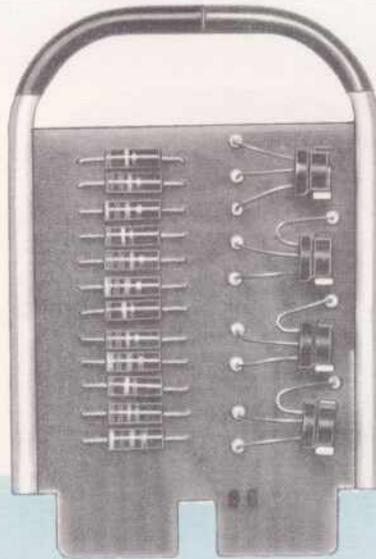
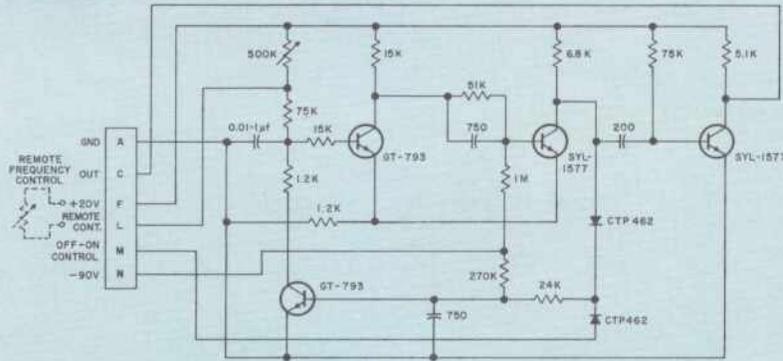
NOTE:
* VALUE DEPENDS ON TRIGGER LEVEL DESIRED.



FREE RUNNING MULTIVIBRATOR, MODEL OM-102. Model OM-102 provides a train of pulses each of which is 10 μ sec wide with a 2 μ sec rise time. The frequency is variable between d-c and 5 kc. With a single value of timing capacitor, the ratio of highest to lowest frequency is 7.5:1. A remote frequency control may be used. At any given frequency setting, maximum time variation between pulses is 10% of that frequency. Pulse frequency can be held to a closer tolerance on special order. The pulse train may be interrupted by any standard M-PAC. Power requirements: +20 volts at 9 ma, -90 volts at 0.43 ma.

UNIT PRICE \$49.00

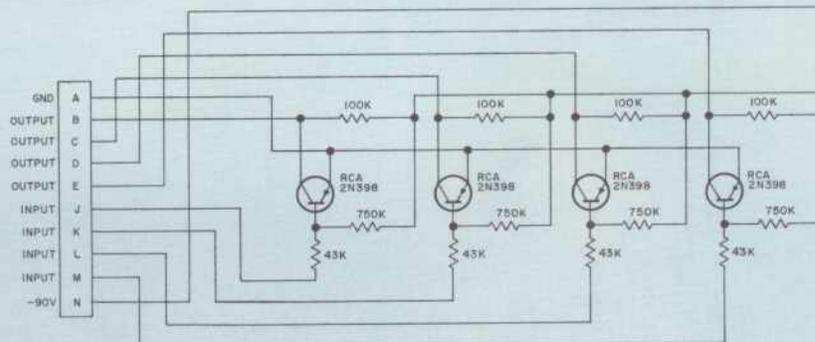
MODEL OM-102



INDICATOR AMPLIFIER, MODEL LA-101. Each Model LA-101 contains 4 individual driver circuits. Each circuit can drive one standard neon indicator assembly that includes a bulb and a 100K series resistor. These circuits can be driven either by a flip-flop or gate output. The driver turns the indicator ON when the input voltage is less than 2 volts, OFF when the input voltage is greater than 8 volts. Power requirements: -90 volts at 1.5 ma for each circuit.

UNIT PRICE \$35.00

MODEL LA-101





Pulse

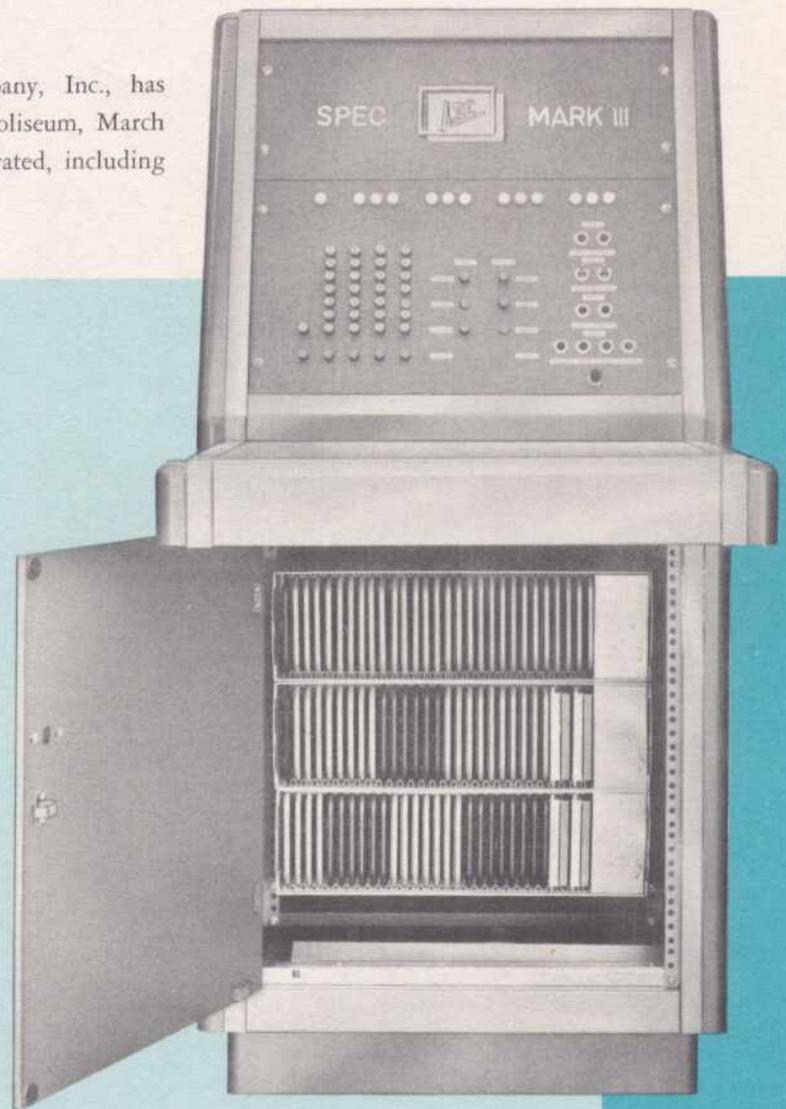
As previously mentioned, 3C PULSEs are written for you, the busy reader. To assist in rapid scanning, topics are purposely kept very brief. Do not hesitate, however, to write for additional information and details. It will be a pleasure to send them along to you.

SEE US AT THE I.R.E. SHOW. Computer Control Company, Inc., has been assigned booths 3308 & 3310 in the New York Coliseum, March 21-24, 1960. Current and new products will be demonstrated, including SPEC, our popular and versatile computer that tutors.

ELECTRONIC DESIGN — NOVEMBER 11, 1959

Did you see the article on pages 80 and 81 covering 3C's Plugboard Logic Computer? SPEC is designed for designers and can be used as a general purpose computer or as a digital differential analyzer. The article comments that "The computer should prove valuable for teaching engineers logical design and implementing the designs of more experienced engineers". Incidentally, it is interesting to note SPEC contains 3 T BLOCs, housing 82 T-PACs (47 are LE-10s), and 4 SM-10 memory units. Each of the latter will store 32 words in a circulating loop at a one megacycle pulse repetition rate. Total bit capacity per circulating line is 416 bits. SPEC's T-PACs incorporate a total of 279 transistors and 1617 diodes.

One of SPEC's major features is the availability of all possible logical implementation at the plugboard. This facilitates the selection of either a general purpose computer or digital differential analyzer. The complete logical design of SPEC can be changed merely by the insertion of different pre-wired plug boards.



STORED PROGRAM EDUCATIONAL COMPUTER



COMPUTER CONTROL COMPANY, INC.

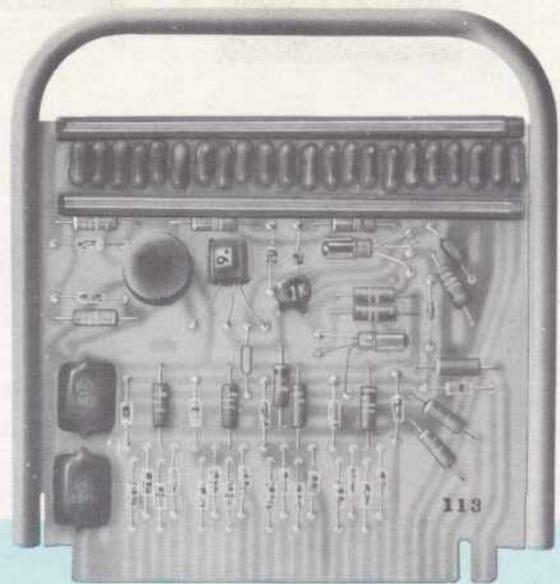
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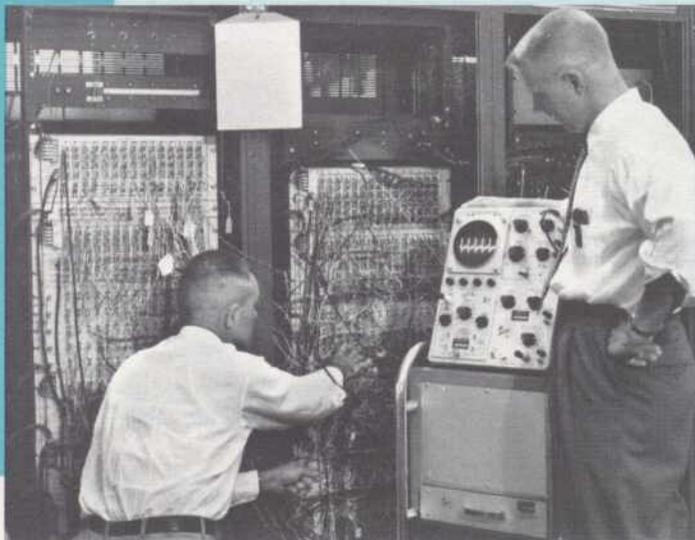
LOGICAL ELEMENT LE-10 (T-PAC, ONE MEGACYCLE)

One of our most popular T-PACs, it serves as a fundamental package type for any digital system. As evidence of its versatility it can handle all 256 functions (82%) of the 65,536 functions of 4 binary variables, and many functions of 5 or more binary variables as determined by the available input logic.

The LE-10 can serve any one of a variety of purposes, among which are the following: Amplifier, Inverter, Driver, Buffer, Flip-flop, Counter Stage, Multiple-coincidence Gate, Frequency Divider, Half-adder, Shift Register Stage and Pattern Generator. It is priced at \$115.00.



T-PAC LOGICAL ELEMENT, Model LE-10



The University of Michigan's Dr. Norman Scott (left) demonstrates the Michigan Instructional Computer, only unit of its kind in the world, to Strand Engineering Company's Robert Carson, who is working for his Ph.D.

Illustration reprinted with kind permission of the University of Michigan and Detroit Edison.

The above, showing the back of the University of Michigan's Instructional Computer, illustrates an earlier vacuum tube series of 3C digital modules (V-PACs) designed, produced and marketed by Computer Control Company, Inc. These have proven their reliability since installation early in 1956.

May we remind you that 3C not only designs and manufactures transistorized digital modules, but that it

also develops and builds a variety of digital systems to suit customers' specific requirements. For example, Universal Tape to Tape Converters, Information Retrieval Systems, Computer Input-Output Systems, Automatic Decoder and Item Tabulators, Digital Comparators, Digital Monitoring Systems, Information Retrieval Systems, Range Time Coders, Radio Telescope Directors, Radio Telescope Readout Systems, High Speed Random Access All-Transistor Magnetic Core Memories, Digital Directors for Automatic Milling Machines, and many others.



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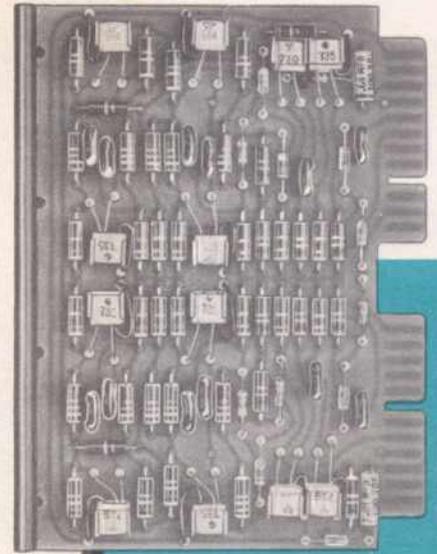


Pulse

NEW M-PAC: SYNCHRONIZER, MODEL SY-101

The SY-101 is a double M-PAC designed either to synchronize random inputs to a clock, or to receive random parallel inputs and to deliver these serially to a counter. Each SY-101 package contains two identical synchronizer circuits. Up to six SY-101 packages may be grouped to allow accumulation of signals from 12 asynchronous sources for delivery to a single counter. Maximum synchronizing rate for an individual circuit is 30 kc, for a group of n circuits 30 kc/n.

Auxiliary circuits available for use with the SY-101 are the OM-102 clock source, the BD-101 decade counter and several other M-PACs.



SPECIFICATIONS

RANDOM INPUT

Frequency..... (30 kc/n) maximum where n is number of random inputs to be synchronized
Amplitude..... +5 to +15 volts
Rise Time..... <20 microseconds
Width..... 5 to 300 microseconds

SYNCHRONIZED COUNT OUTPUT

Amplitude..... +8 to +15 volts
Rise Time..... 2 microseconds maximum
Width..... 5 microseconds ±15%

SHIFT INPUTS

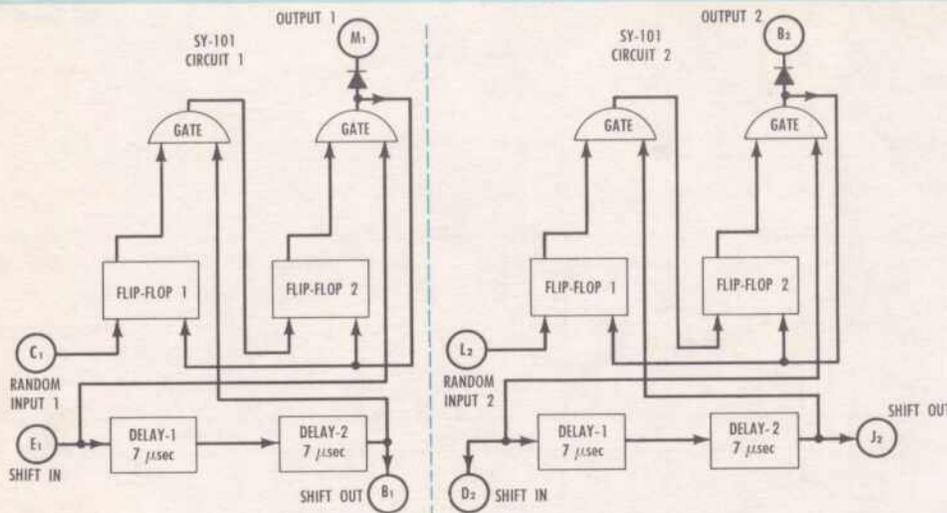
Frequency..... Min. twice the random input frequency
 Max. $\frac{n}{60 \text{ kc}}$
Amplitude..... +15 to +20 volts
Rise and Fall Time..... 2 microseconds maximum
Width..... 8 microseconds ±10%

SHIFT OUTPUTS

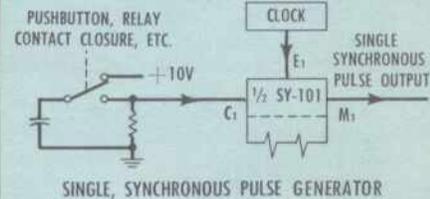
Frequency..... Same as shift inputs
Amplitude..... +15 to +20 volts
Rise Time..... 4 microseconds max. (unloaded)
Fall Time..... 2 microseconds (max.) (unloaded)
Width..... 7 microseconds ±15%

Power Requirements..... +20 volts d-c, ±10% at 35 milliamperes
 -90 volts d-c, ±10% at 1 milliampere

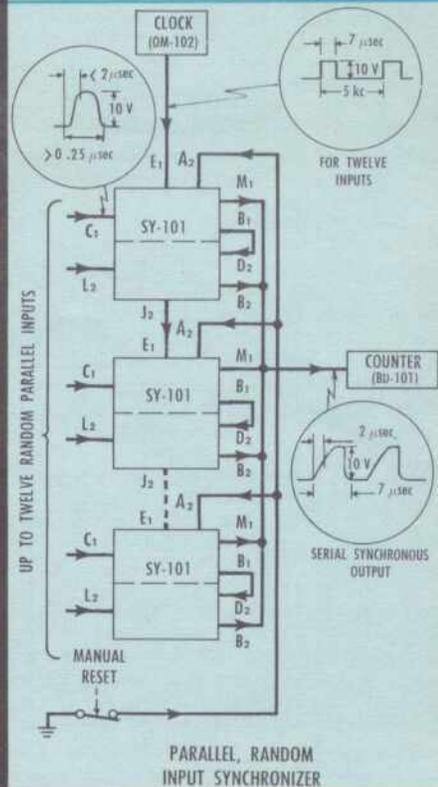
UNIT PRICE \$77.00



APPLICATIONS



SINGLE, SYNCHRONOUS PULSE GENERATOR



PARALLEL, RANDOM INPUT SYNCHRONIZER



COMPUTER CONTROL COMPANY, INC.

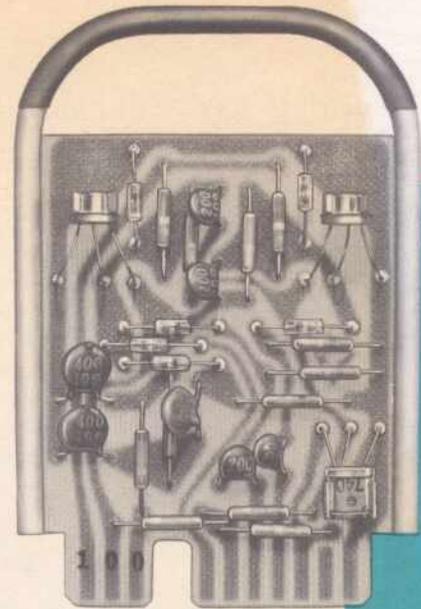
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SHIFT FLIP-FLOP Model SF-101

The 3C-PAC Model SF-101 shift flip-flop employs an Eccles-Jordan D.C. cross-coupled circuit. The transistors are operated at cut-off or saturation resulting in output swings of approximately 15 volts. It is intended specifically for use as a shift register stage. In conformance with the requirements of this usage the following circuitry features have been designed into the Model SF-101:

- Set input has a built-in RC network to provide an effective delay of the carry pulse from the preceding stage of approximately 2.0 microseconds.
- An additional set input is provided to facilitate either parallel or serial input of data into the shift register.
- An emitter follower output circuit is provided to facilitate either parallel or serial output of data from the shift register. This output can drive up to ten diode gate inputs.
- An A.C. coupled shift input permits shifting of up to ten stages by the Pulse Amplifier Model PA-104.
- A clear or reset input is provided for initial resetting or bulk clearing of the shift register. The Clear Input can be driven by switch contacts or by the Inverter Amplifier Model IA-104.
- Shift registers with any number of stages can be implemented using the Model SF-101 3C-PAC without requiring intervening circuitry or components between stages.

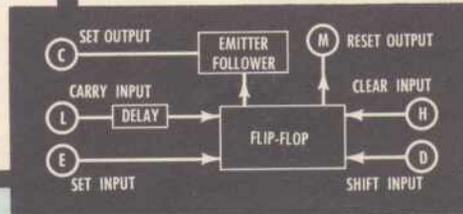


MODEL SF-101

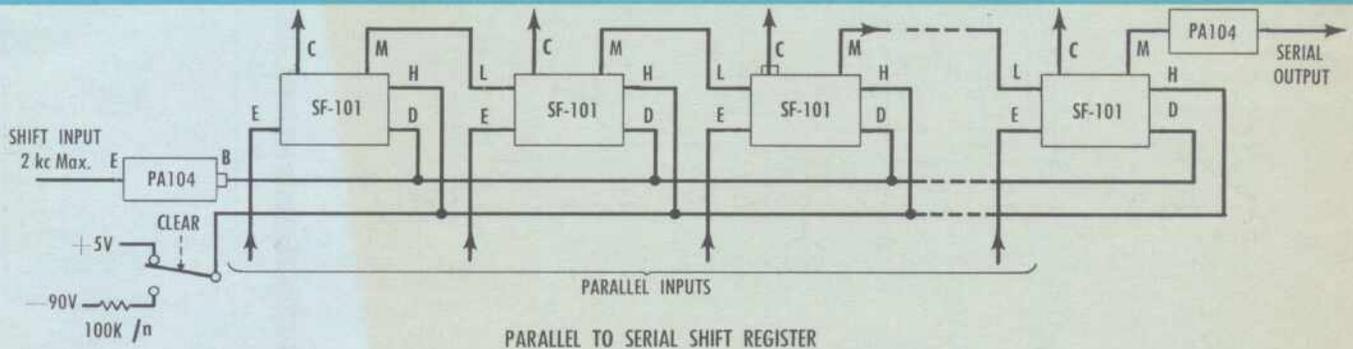
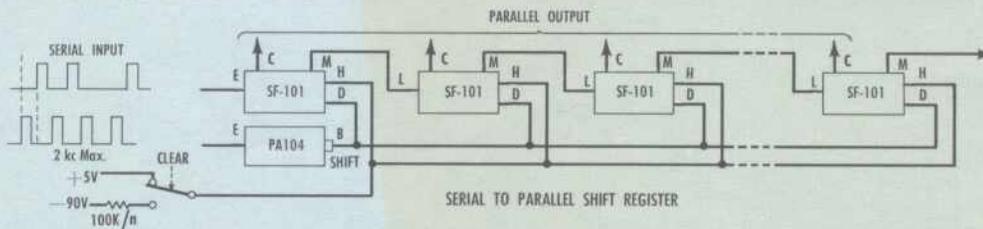
SPECIFICATIONS

Shift Rate	D.C. to 2 Kilocycles
Shift Input Amplitude	10 volts nominal
Shift Input Duration	2 microseconds
Collector Swing	15 volts
Clear Input Minimum Duration	50 microseconds
Current From +20 volt supply	5.0 ma.
Current From -90 volt supply	0.5 ma.

PRICE: \$33.00 (INCLUDES CONNECTOR AND GUIDE PIN)



APPLICATIONS



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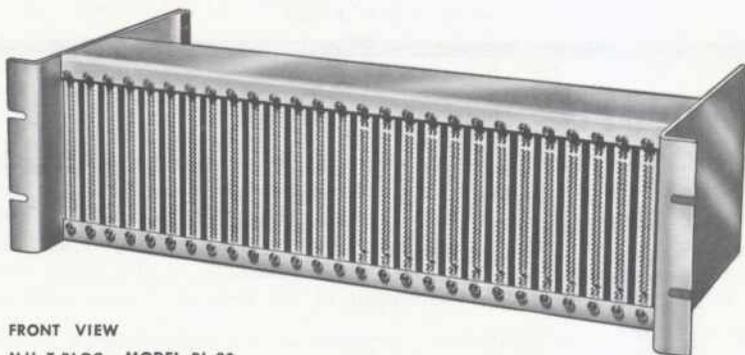
Pulse

3C PRESENTS THE NEW MIL-T-PAC SERIES

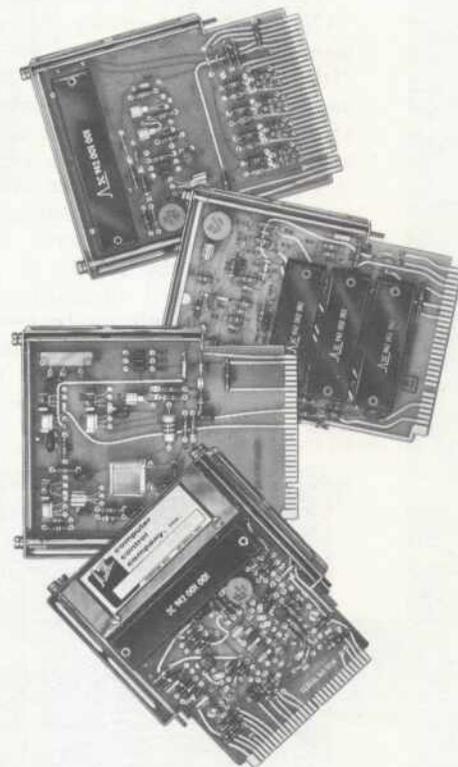
3C presents a completely new series of dynamic, 1 megacycle, digital modules, specifically designed and constructed for Military systems and applications. Built to Military Specification MIL-E 16400, these new packages are logically and functionally equivalent to our well-known 1 megacycle T-PAC series, but differ considerably in format.

The new MIL-T-PACs withstand Type 1 vibration and Class A shock and are guaranteed to exceed Class 4 temperatures specified in MIL-E 16400. Under actual test they have performed satisfactorily in the zero to +65°C range. All delay lines and pulse transformers are encapsulated. Military components of preferred values have been used throughout.

The cards consist of glass base, laminated sheets, fiberglass epoxy printed circuit boards and measure $6\frac{3}{8}$ inches deep by $5\frac{1}{4}$ inches high. The double fingers are nickel-rhodium plated in accordance with Military Specification. Each card is riveted to a stainless steel frame which protects the mounted components from accidental damage during insertion or withdrawal. The frame serves as a positioning guide during insertion. Captive bolts, mounted within the frame, securely fasten each MIL-T-PAC to the MIL-T-BLOC.



FRONT VIEW
MIL-T-BLOC MODEL BL-20



- ▶ LOGICAL ELEMENT Model LE-20
- ▶ STORAGE LINE (double package)
Model SL-20
- ▶ UNIT DELAY LINE (4 unit delays)
Model DP-20
- ▶ MASTER OSCILLATOR Model OC-20
- ▶ SLAVE CLOCK Model SC-20
- ▶ SYNCHRONOUS GENERATOR Model SG-20
- ▶ STATIC FLIP-FLOP Model FS-20

The above packages currently comprise the MIL-T series. Additional packages will be added.



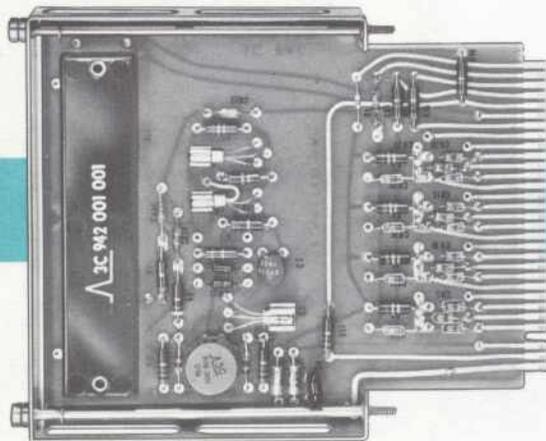
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LOGICAL ELEMENT Model LE-20

This is the basic unit of the MIL-T-PAC series. It is a dynamic decision-making element which performs logical functions determined by external connections. Information is represented by the presence or absence of pulses at a basic repetition rate of 1 megacycle per second.

This MIL-T-PAC contains four (4) four-leg "AND" gates, each leg being available on the terminal. The gate outputs are mixed in a four-leg "OR" structure, reshaped by standard clock pulse, amplified, and made available one microsecond after the input signals have occurred. The package output is presented on two separate lines as negative pulses on the assertion output, and as positive pulses on the negation output. Either output line may be directly connected to its own package inputs, or to the inputs of any other package. Additional logical flexibility is provided by an inhibit input which can be used to control (on-off) the output of the gate structure. Also, three of the gate outputs are brought out to the terminal, and by wiring them together, an eight or twelve legged gate can be formed.



MODEL LE-20 FRONT VIEW

POWER REQUIREMENTS:

-12 volts d-c $\pm 10\%$, 20 ma (full duty factor)
+12 volts d-c $\pm 10\%$, 10 ma (for max loading only)

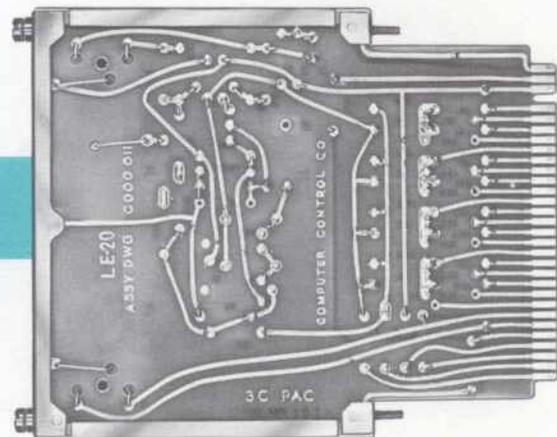
INPUTS:

	ASSERTION	NEGATION	CLOCK
Amplitude (Relative to Ref. Level)	Nom. -4V Min. -1.5V Max. -20V	+4V +1.5V +10V	-3V -1V -10V
Reference Level	GND		GND
Pulse Width (Microsec.)*	>0.3	>0.3	0.20, $\pm 10\%$
Source Impedance	<200 ohms	<200 ohms	
Repetition Rate			1000 kc $\pm 0.5\%$

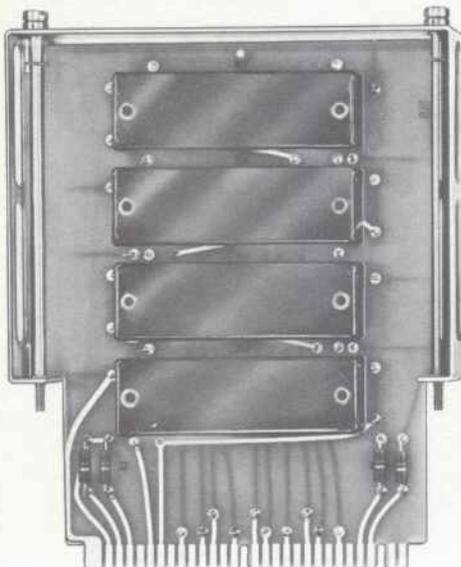
*Pulse Width measured at 10% amplitude. Signal inputs must be synchronized so that they have the specified amplitude in coincidence with a 1 Mcs. synchronizing pulse input.

OUTPUTS:

	ASSERTION	NEGATION
Amplitude (Relative to Ref. Level)	Nom. -5V Min. -3V	+5V +3V
Reference Level	GND	
Pulse Width (Microsec.)*	0.4, -15% +25%	0.4, -15% +25%
Rise & Fall Time (Microsec.)	Less than 0.15	Less than 0.15
Source Impedance	120 ohms	120 ohms
Maximum Loading	9 gate legs & 5 unit delays or 20 gate legs with "pull-up" resistor connected to +12V	20 gate legs & 5 unit delays



MODEL LE-20 REAR VIEW



MODEL DP-20

UNIT DELAY LINE Model DP-20

The basic element is an electrical delay of exactly one pulse period (one μsec), and provides timing or delay of either assertion or negation LE-20 output signals. The package includes four individual one-pulse-period delay lines and two assertion and two negation terminating resistors. The impedance of the delay lines is 120 ohms to match the output of the logical element package.

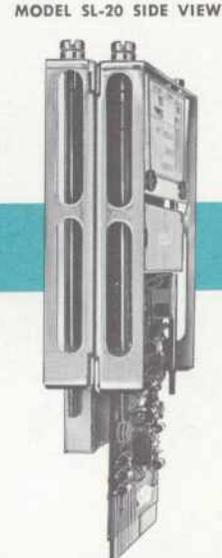
In any series delay line configuration, partially delayed signals are available at the extra terminals along the delay path. Signals may flow in either direction through the delay line and either assertion or negation signals can be delayed.

INPUT:

Accepts the output of either the LE-20 or SL-20 3C-PACs.

OUTPUT:

Delay (per element)	1.00 μsec , $\pm 2\%$
Cut-off Frequency	5.6 mc
Impedance	120 ohms
Attenuation	<10% μsec



STORAGE LINE Model SL-20

The Storage Line SL-20 is a single 3C-PAC containing both a serial memory and a logical element. The memory section has a driver, magnetostrictive delay line and an output amplifier. With the exception of the input gating logic, the logical element section is identical to that of the LE-20 LOGICAL ELEMENT. A single SL-20 MIL-T-PAC will delay signals to a maximum of 1000 microseconds. Two or more can be cascaded to obtain greater delays.

POWER REQUIREMENTS:

-12 volts d-c: $\pm 10\%$ at 60 ma full duty, -4 volts d-c: $\pm 10\%$ at 1 ma.

INPUT (Negation)

Amplitude	Nominal: +3 volts
	Min. +1.5 volts
	Max. +10.0 volts
	(Capacity Coupled)
Reference Level	0.4 μ sec $\pm 15\%$
Pulse Width	<0.15 μ sec
Rise & Fall Time	1000 ohms
Impedance (input)	+0.5 volts
Allowable Noise	1 mc $\pm 0.5\%$
Repetition Rate	

OUTPUT:

	ASSERTION	NEGATION	MEMORY SECTION
Amplitude	Nom. -5 volts	+5 volts	-4
(Relative to Ref. Level)	Min. -3 volts	+3 volts	
Reference Level	GND	-1.5 volts	GND
Pulse Width*	0.4 μ sec -15% +25%	0.4 μ sec -15% +25%	0.6 $\pm 40\%$
Rise & Fall Time	<0.15 μ sec	<0.15 μ sec	<0.2
Impedance	120 ohms	120 ohms	$\sim 150\Omega$
Maximum Loading	10 gate legs and 5 unit delays	20 gate legs and 5 unit delays	3 gate legs
	or 20 gate legs with "pull-up" resistor connected		

*See description under LE-10

OSCILLATOR CLOCK Model OC-20

The OC-20 is a 1000 kc crystal-controlled oscillator and driver. It contains both a master oscillator and a slave clock circuit. The OC-20 can drive up to 20 SC-20 Slave Clocks.

POWER REQUIREMENTS:

-12 volts d-c $\pm 10\%$ at 30 ma

INPUT:

The OC-20 requires no input other than the power requirements mentioned above.

OUTPUT: (of Master Oscillator)

	UNLOADED	FULLY LOADED
Width (at 10% amp)	Nom. 0.6 μ sec	0.6 μ sec
Rise Time	<0.05 μ sec	<0.1 μ sec
Reference Level	-12 volts	-12 volts
Frequency	1000 kc $\pm 0.02\%$	1000 kc $\pm 0.02\%$
Amplitude	12 volts	11 volts
Maximum Load		20 SC-20 PACs

SLAVE CLOCK Model SC-20

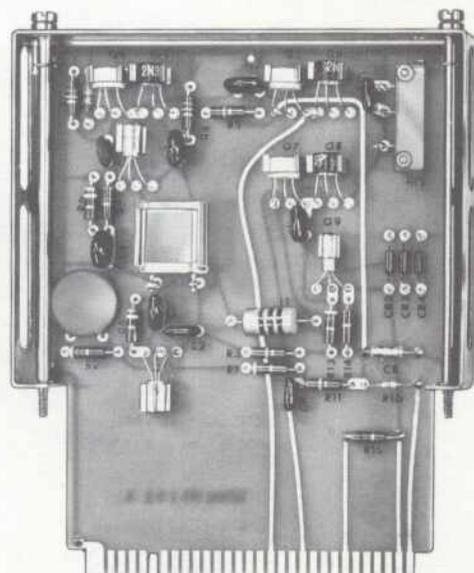
This is a three transistor amplifier which supplies clock pulses for one MIL-T-BLOC. It consists of a Slave Clock circuit only.

POWER REQUIREMENTS:

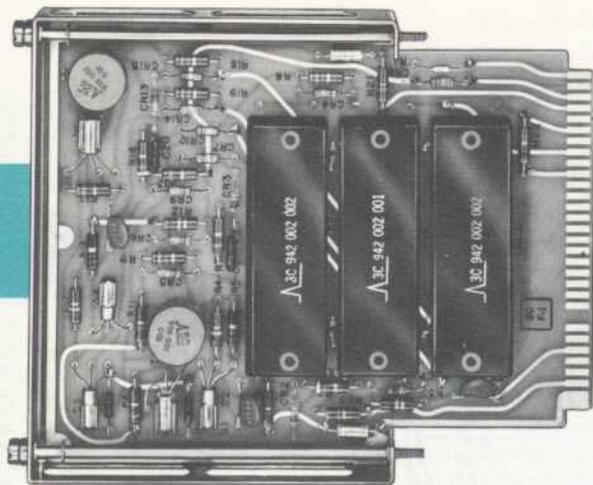
-12 volts at 10 ma

OUTPUT:

Amplitude	Min. -2 volts
	Nom. -3 volts
	0 volts
Reference Level	
Width	0.2 μ sec $\pm 10\%$ (at -0.5v)
Maximum Load	29 LE-20 or equiv.



MODEL OC-20



MODEL SG-20

SYNCHRONOUS GENERATOR Model SG-20

The purpose of the Synchronous Generator SG-20 is to accept randomly-timed, arbitrarily-shaped input pulses, such as might be obtained from a magnetic tape read amplifier, a paper tape reader, a keyboard, relay, or switch, and to convert them into one and only one properly-timed and shaped pulse compatible with standard wave forms used in the MIL-T-PAC series. Assertion and Negation outputs are provided similarly to the LOGICAL ELEMENT LE-20.

INPUT:

Amplitude	+10 V (nom) +100%, -50%
Pulse Width	>0.25 μ sec
Rise Time	1 μ sec/volt or less
Frequency	250 kc maximum
Impedance	5000 ohms (AC coupled)
Allowable Noise	< +2 volts from base line
Duty Factor	50% maximum

OUTPUT:

	ASSERTION	NEGATION
Amplitude	Min. -3V	+3V
Impedance	120 ohms	120 ohms
Reference Level	GND	-1.5 volts
Maximum Loading	9 gate legs and 5 unit delays or 20 gate legs with "pull-up" connected	20 gate legs no unit delays

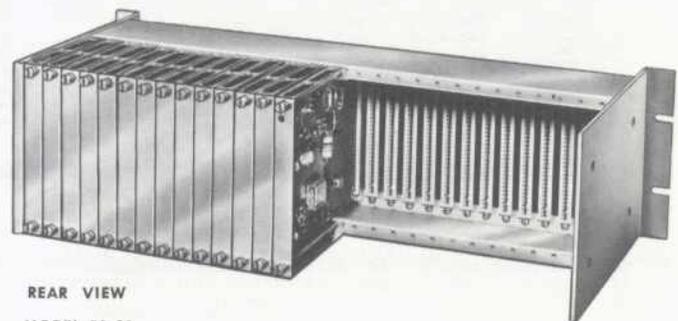
STATIC FLIP-FLOP Model FS-20

The package contains 2 independent Eccles-Jordan flip-flop circuits. It may be used to implement a variety of functions such as a logical element, an output package, as a relay driver and in shift register

applications. Each flip-flop has gated inputs and set and reset outputs. The maximum turnover rate is in excess of one megacycle. Additional information on the FS-20 will be announced at an early date.

MIL-T-BLOC Model BL-20

Built of aluminum, clear anodized, it measures 19" wide by 5 $\frac{1}{4}$ " high by 8" deep and accommodates 27 single MIL-T-PACs. It is notched to fit any standard size rack. The front panel, can be supplied with a taper pin plugboard format or solder type connectors. A rear view of the MIL-T-BLOC shows the shoulders which are drilled and tapped to accept the captive retention bolts supplied with each MIL-T-PAC. Thus, each module is securely held in position and in positive contact with its connector. Self locking thread inserts assist in achieving this even under vibration and shock conditions. The BL-20 requires an independent power supply.



REAR VIEW
MODEL BL-20

AVAILABLE ON SPECIAL ORDER

- Gold Plated Printed Circuits
- Two Part Connectors
- Anodized Aluminum Frames
- MIL-T-PACs for Operation at Higher Frequencies and Temperatures
- MIL-T-PACs for Special Applications
- Special Purpose Digital Systems Designed and Built to Military Specifications
- 3C will gladly quote on any of the above. Proposals submitted on request.



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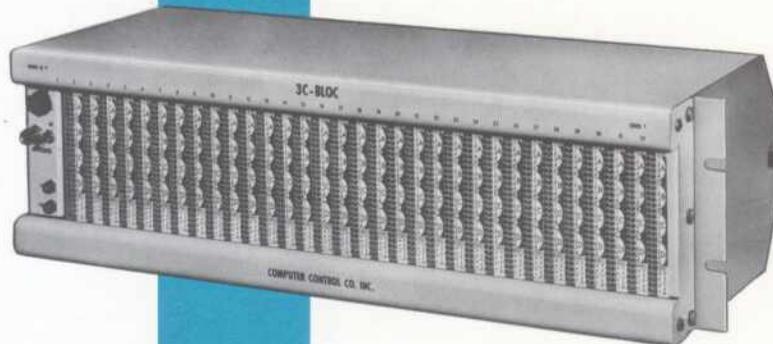
FOUR NEW ADDITIONS TO 3C's T-PAC SERIES

3C announces the addition of T-BLOC Model BL-11, Power Supply Model RP-10, Oscillator Clock Model OC-10 and Slave Clock Model SC-10 to its well-known line of dynamic, one megacycle, T-PAC digital modules.

These four new components have been designed for the special purpose digital system where centralized controls, a centralized power supply, and additional T-PAC slot accommodations are desired. The combination offers attractive cost savings to the user. Only one power source is required rather than the separate ones built into each Model BL-10 T-BLOC. The BL-11 holds 3 more T-PACs than the BL-10 plus an Oscillator or Slave Clock Module without any increase in overall measurements.

T-BLOC MODEL BL-11

The BL-11 is standard size, notched for standard rack mounting, and measures 5 1/4" x 19" x 8" overall. 32 T-PAC slots are provided plus a space for an Oscillator or Slave Clock module. The front panel carries a taper pin plugboard where all signal interconnections are made. Multicolored plastic inserts identify the plugboard connections. They also offer a convenient means of identifying T-PAC usage within the system. Located to the left of the plugboard is a power ON switch with indicator light, a miniature connector and plug for an external power source and clock input. A hold-down bar assures mechanical contact between the T-PAC and the connector and positive retention against shock and vibration. Turning two knurled thumb screws enables the hold-down bar to be quickly removed from the T-BLOC chassis. All T-PACs are inserted from the rear. Power for the BL-11 must be provided externally either by RP-10 or an equivalent power source.



NEW T-BLOC MODEL BL-11
FRONT VIEW SHOWS TAPER
PIN PLUGBOARD PANEL



REAR VIEW — HOLDS 32 T-PACs PLUS
OSCILLATOR OR SLAVE CLOCK PACKAGE



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POWER SUPPLY MODEL RP-10

The Power Supply Model RP-10 is a completely transistorized, regulated, 8 ampere power source especially designed and conservatively rated for computer applications. It has been designed for standard rack mounting, measures 5 1/4" x 19" x 11 1/2" and will power 9 fully loaded BL-11s. It requires a two inch clearance in front of the mounting surface, weighs 38 lbs. and will operate in ambient temperatures from -10° to +55° Centigrade.

The basic model provides a -16 volts d-c required for systems using 3C's T-PACs. A voltmeter and ammeter are furnished with full-scale ranges of 25 volts and 10 amperes respectively. The output voltage is variable ±15% from nominal for marginal checking purposes.

Provision is made for the optional addition of a low power plug-in supply to furnish a different

voltage at low current. This may be a low positive voltage frequently used in T-PAC systems, or a -90 volt d-c supply to operate neon indicators. A circuit is included to blow the power supply fuse if the out-put voltage rises above 20 volts. This will protect transistors in the load PACs from high voltage in the event of a malfunction in the RP-10. The RP-10 will supply -16 volt power for 320 LE-10s, operating at 1 mc continuously, 640 LE-10s operating at a maximum duty cycle of 50%, 265 FS-10s, or any combination which satisfies the relationship.

$$.025 \alpha N_{LE} + .03 F_S = 8 \text{ amperes}$$

where α = max. duty cycle at which LE-10s will operate

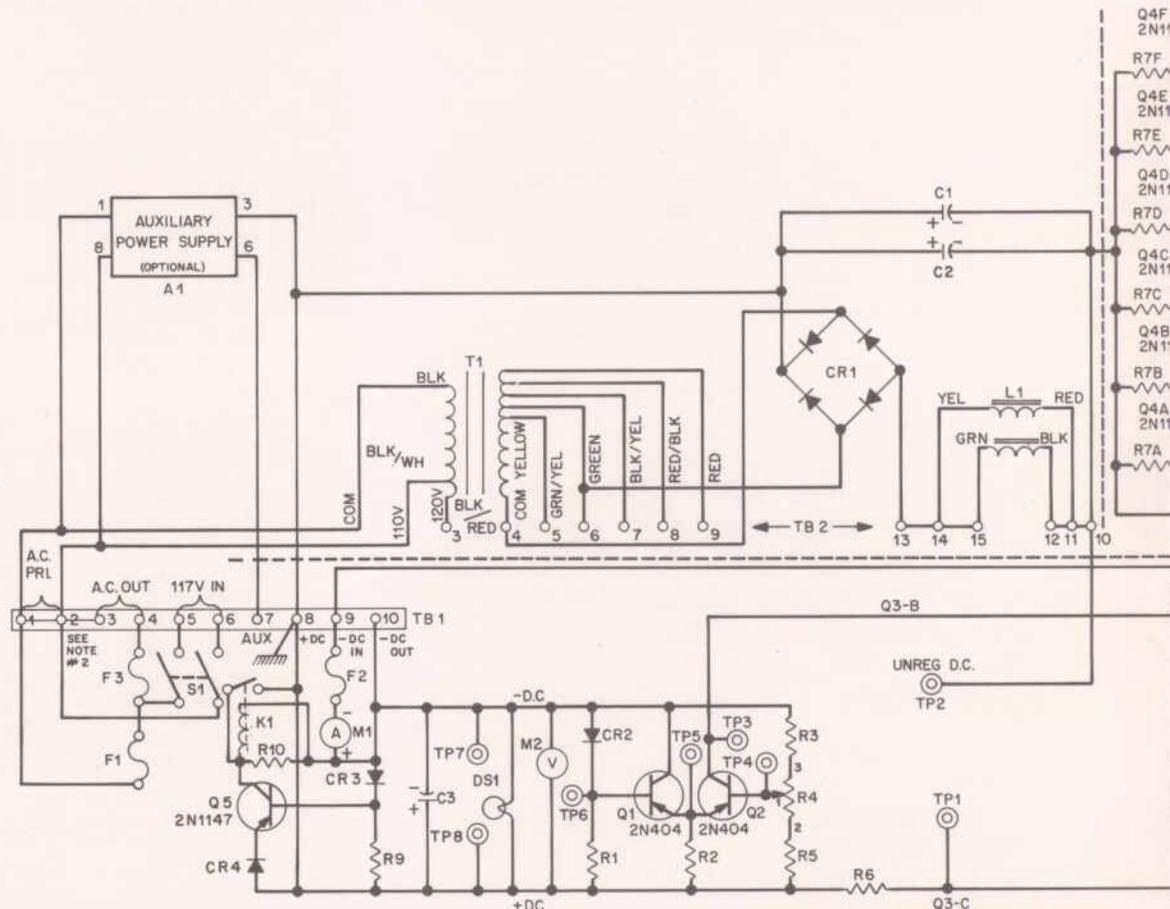
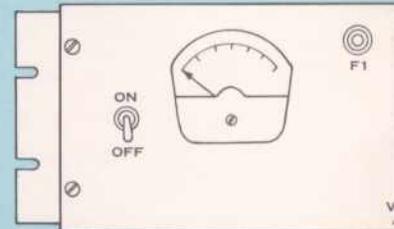
If other less frequently used PACs are included, the current consumed by them must be subtracted from the 8 amperes.

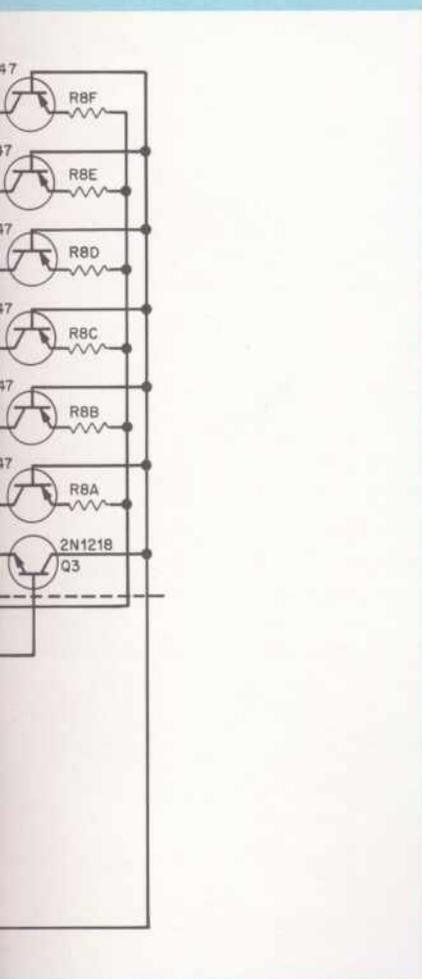
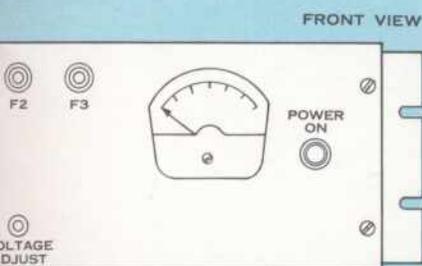
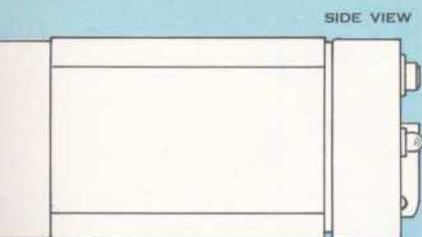
SPECIFICATIONS :

POWER REQUIREMENTS:

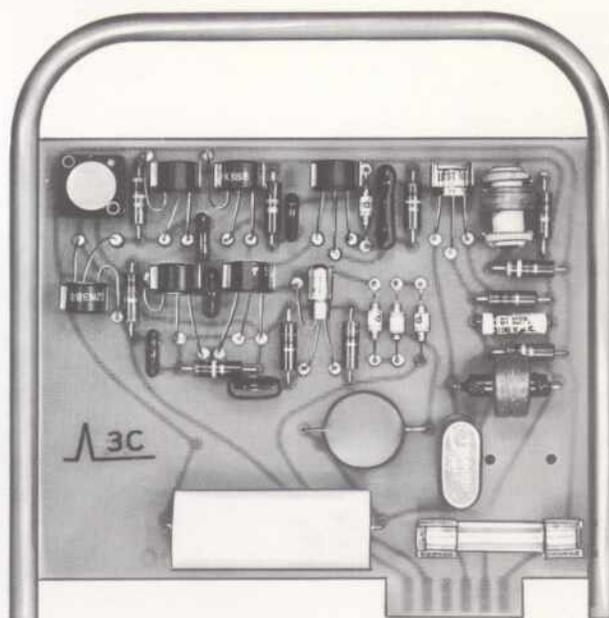
Input voltage: 117 volts ±10%
Frequency: 60 cycles, single phase

Output voltage: 16.0 volts
Temperature Coefficient: 3 mv/°C
Adjustment Range: 13 to 19 volts
Load Current: 1 to 8 amps
Ripple: 2 mv., max.
Internal Impedance: .01 ohms
Regulation against line voltage, 105-129 v.: .03 volts





OSCILLATOR CLOCK, MODEL OC-10



The Oscillator Clock, Model OC-10 plugs into a six contact etched circuit connector at the rear of the BL-11 control panel. It provides 1 mc clock pulses to one BL-11 and synchronizing drive from 1 to 14 Slave Clocks Model SC-10. The OC-10 occupies the space provided for it in the BL-11 which leaves room for 32 packages.

SPECIFICATIONS :

POWER REQUIREMENTS: OC-10 -16 volts d-c, $\pm 10\%$; 25 ma.

SYNC DRIVE OUTPUT	Unloaded	14 BLOC load
	Amplitude:	14.5 volts, $\pm 5\%$
Width (at 10% amp):	0.3 μsec , $\pm 10\%$	0.65 μsec , $\pm 10\%$
Frequency:	1,000 kc, $\pm 0.02\%$	1,000 kc, $\pm 0.02\%$

SLAVE CLOCK, MODEL SC-10

The Slave Clock, Model SC-10 is an identical package to the OC-10, but without the crystal controlled oscillator components. It incorporates a fuse in series with the -16 volt supply to protect the T-BLOC. By-pass capacitors in the circuits filter high-frequency currents from the -16 volt supply. The SC-10 uses the same space in the BL-11 which is reserved for the OC-10.

SPECIFICATIONS:

POWER REQUIREMENTS:	SC-10	-16 volts d-c, $\pm 10\%$; 6 ma.
CLOCK OUTPUT	Unloaded	Loaded
	(32 LE-10s reset)	(32 LE-10s full duty)
Amplitude:	2.8 volts, $\pm 20\%$	2.0 volts, $\pm 25\%$
Width, T (at 0.5 v level)	Set to 0.2 μ sec	0.25 μ sec, $\pm 10\%$



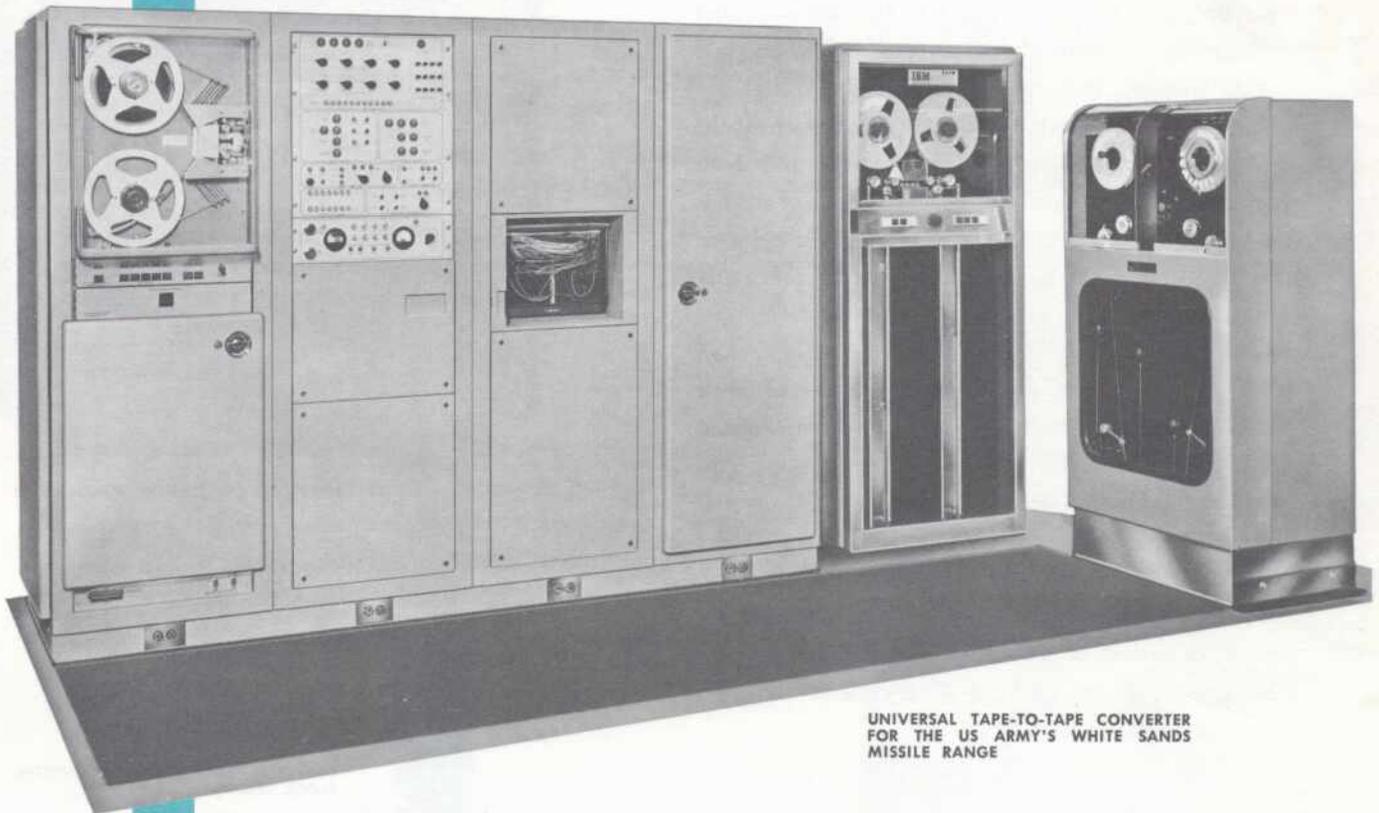
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A UNIVERSAL TAPE TO TAPE CONVERTER



UNIVERSAL TAPE-TO-TAPE CONVERTER
FOR THE US ARMY'S WHITE SANDS
MISSILE RANGE

A recent interesting development by 3C is a digital tape to tape language translator. The initial system has been designed specifically for the United States Army's White Sands Missile Range.

It accepts, as input, the digital magnetic tapes from radar, telemetering and other instrumentation, and converts the output data into a magnetic tape with a format suitable for input to the IBM 650, IBM 704, and UNIVAC Scientific 1103A high speed computers. Furthermore, inherent flexibility permits it to handle various forms of magnetic recording ; such as serial or parallel recording, binary or decimal notation, differences in tape speed and recording density, and other variables. It will also convert between the languages and formats of IBM and UNIVAC in either direction.

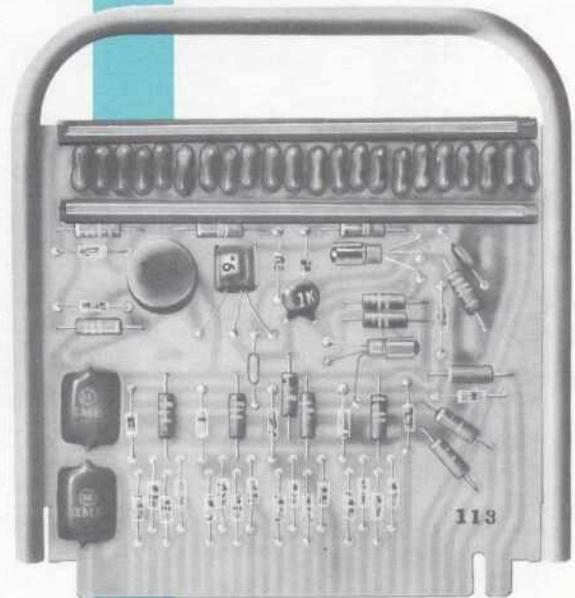


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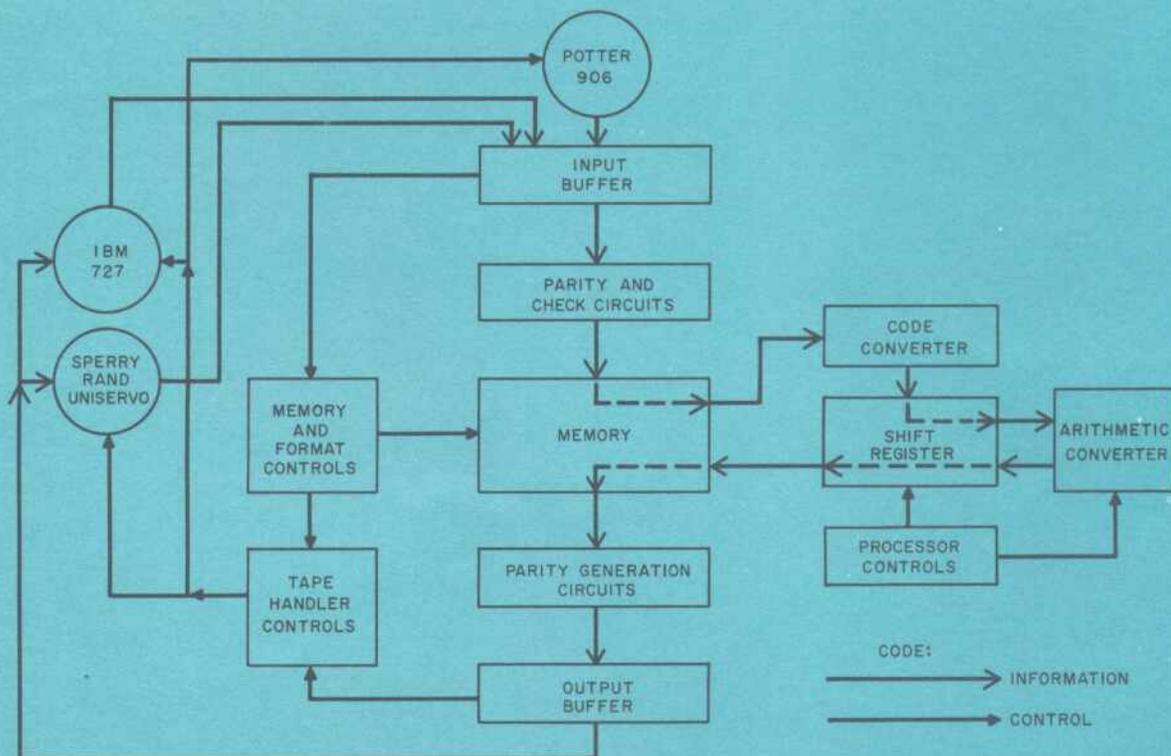
The Universal Tape to Tape Converter has provisions for full control over code conversion, word length, character placement within the word, block length, word arrangement within the blocks, suppression or selection of input blocks, serial-parallel rearrangement, error checking, error correction, and other features. It is capable of handling continuous data tapes, tapes with or without sprocket channels, tapes with various inter-block spacing, and both return-to-zero and non-return-to-zero forms of recording. These and other special characters are relevant to its use with the high speed computers previously mentioned.

The high degree of flexibility is achieved by a modular design which utilizes 3C's transistorized T-PAC 1 megacycle dynamic digital modules. Approximately 600 T-PACs are used in the overall system. 300 of these are the Logical Element, Model LE-10. The UTTC also contains a 3C Random Access Magnetic Core Memory with a word capacity of 2048 words at 8 bits per word. The memory has an 8.0 microsecond Read-Write cycle *.



T-PAC LOGICAL ELEMENT MODEL LE-10

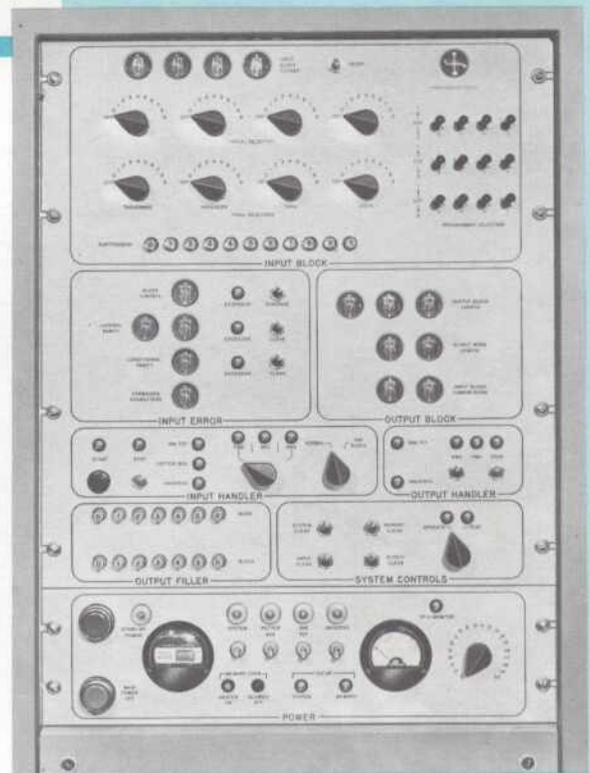
UNIVERSAL TAPE-TO-TAPE CONVERTER
BLOCK DIAGRAM





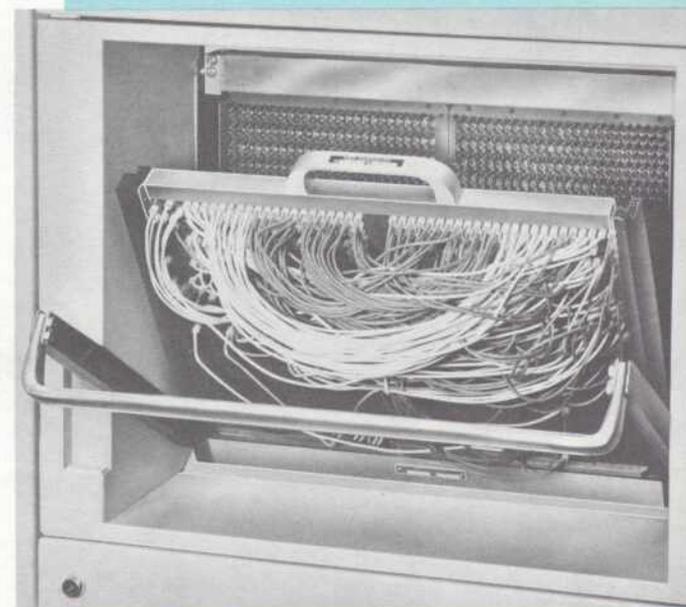
The basic Universal Tape to Tape Converter design is inherently flexible. Numerous modifications and extensions of it are conceivable. For instance, it could be adapted to handle other inputs such as punched cards, paper tape, inputs from a manually operated keyboard, etc. Its output may be fed directly into printers, paper tape punches, plotters, and other output devices. There are many potential applications for these various types of data translation in business and industry. A typical one might involve sales transactions of a multi-branch organization. These could be recorded on paper tape by an Add-punch at each branch and transmitted weekly to a central location. Processed there by a Paper-Tape-to-Magnetic-Tape-Converter into an acceptable input, further detailed analysis is then made by a high speed computer (IBM 650 or similar). Very considerable cost savings are possible with such an application together with almost immediate availability of detailed sales statistics.

Another application is that of a High Speed Collator for rapid information storage in a magnetic tape file. An IBM type card Reader-Punch provides access. The reading section conveys information to the digital system. IBM input cards contain the argument or address, of information to be modified or examined, instructions about the modification, or operation to be performed. Modification or replacement data is thus inserted into the file. The punch section of the IBM 519 serves as the system output. Information from the file, in the form of an argument and associated data, is punched out on IBM cards.



THE CENTRALLY LOCATED CONTROL PANEL EMBODIES ALL NECESSARY CONTROLS FOR COMPLETE OPERATION OF THE SYSTEM INCLUDING TAPE UNITS.

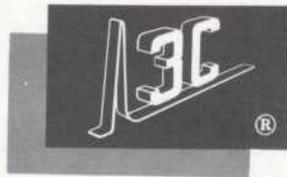
THE PLUGBOARD CARRIES A SPECIFIC PROGRAM INCLUDING TYPE OF CODE CONVERSION, TAPE FORMATS, TAPE UNITS TO BE USED AND OTHER FUNCTIONS. APPROXIMATELY 50 INPUT-OUTPUT COMBINATIONS CAN BE PROGRAMMED WITH IT.



A data Translator for converting analog signals into digital form is a third typical example. It divides input information into proper length tape records for further processing by a high speed computer (IBM 704 or similar). Flexibility is designed into the Digital System (incorporates a magnetic buffering system) whereby it handles the processed data, re-recorded on IBM tape, and reconverts it into an analog signal containing no extraneous distortions.

Since its inception in 1952, 3C has been designing digital systems of all kinds including Special Purpose Computers, Data Converters, Information Storage and Retrieval Systems, Digital Communications Check-out Equipment, Random Access Magnetic Core Memories, etc. Please write us of your needs. Our Applications and Systems Engineers are available for consultation purposes. Proposals will gladly be submitted on request.

**A reprint of a technical article entitled "A Universal Tape to Tape Converter for White Sands Missile Range," by Joseph L. Medoff and Ara A. Aykanian, published in the April 1960 issue of Automatic Control, is available on request.*



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TWO NEW SERIES OF 3C PAC's Announcements will be forthcoming on both within the next 60 days.

THREE IMPORTANT NEW PIECES OF REFERENCE LITERATURE — mail the enclosed reply card for your copy of:

PROCEEDINGS OF DYNAMIC DIGITAL LOGIC CONFERENCE HELD MARCH 1960, BEVERLY HILLS CALIFORNIA. Now on the press, individual copies of the PROCEEDINGS will be made available to those interested. It is a 72 page booklet containing illustrated reprints of the following six papers given at The First Users Conference on Dynamic Digital Logic —

- "The Application of Serial Techniques to Digital Systems" by Robert L. Thomason and Thomas Wong, U. S. Naval Ordnance Test Station, China Lake, California
- "Logical Simulation of Dynamic Systems" by Ray Wolfe, Space Technology Laboratories, Los Angeles, California
- "Application of Digital Techniques in a Meteor Burst Communication System" by H. L. Heibeck, U. S. Navy Electronics Laboratory, San Diego, California
- "709 T-PAC Wiring Program" by Thomas Wong and Robert L. Thomason, U. S. Naval Ordnance Test Station, China Lake, California
- "Six Applications of Dynamic Logic" by Mahlon Easterling and Solomon Golomb, Jet Propulsion Laboratory, Pasadena, California
- "The Use of Serial Techniques in the Design of an Incremental Computer" by Frank E. Brinkerhoff, Computer Control Company, Inc., Western Division, Los Angeles, California.

THE UNIVERSAL TAPE-TO-TAPE CONVERTER A reprint is now available of the complete and illustrated technical article as it appeared in the April 1960 issue of AUTOMATIC CONTROL. Written by Joseph Medoff and Ara Aykanian, it covers the Universal Tape-to-Tape Converter designed and built by 3C for the U. S. Army's White Sands Missile Range (WSMR). Included are three typical WSMR magnetic tape formats, methods of code conversion, functional control, and information flow.

RANDOM ACCESS MAGNETIC CORE MEMORIES Just off the press is a new 8 page illustrated catalog showing three typical Random Access Magnetic Core Memories designed and built by 3C. Dimensions of each are given. It includes general and detailed descriptive material, specifications, description of operation, and a block diagram of a typical 3C Random Access Magnetic Core Memory System.

As mentioned above, please use the enclosed business reply card to obtain copies of any of these publications without charge.

3C'S FORTHCOMING CONVENTION ATTENDANCE Our Western Division at 2251 Barry Avenue, Los Angeles will staff our exhibit at the Western Electronic Show and Convention (WESCON) being held this year at the Los Angeles Sports Arena, August 23-26. They will display, in booths #561 and 562, a selection of our M, T, and MIL-T digital modules, two completely new series of high speed digital modules, and various types of Code Bar Switches. Technical personnel will be on hand to discuss Random Access Memories, Universal Tape-to-Tape Converters, Coordinate Conversion Computers, and other special purpose digital systems.

Scheduled for Oct, 1

Gartner ordered 7 Sept.



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